Contributions to CMS-HCAL Detector

Shashi Dugad

for SiPM Development Group

Annual DHEP Meeting 7-8 April 2016

SiPM Group and its activities

- Large number of Project students from VIIT-Pune
- MTech: P. Rakshe (VITT-Pune)
- JRF: S. Kamthe, A. Kurup, S. Lokhandwala, R. A. Shukla
- J. Freeman (FNAL) , A. Kaminsky (MSU), S. Los (FNAL)
- S.R. Dugad, S. Duttagupta (IIT-B), C.S. Garde (VIIT-Pune), A.V. Gopal, S.K. Gupta, S. Prabhu, R.A. Shukla

Activities:

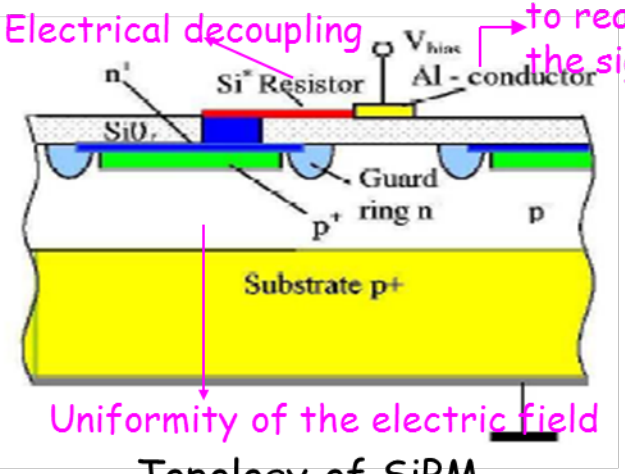
- Development of SiPM and associated electronics
- Application of these developments to various experimental activities and national needs

Activities of SiPM Group

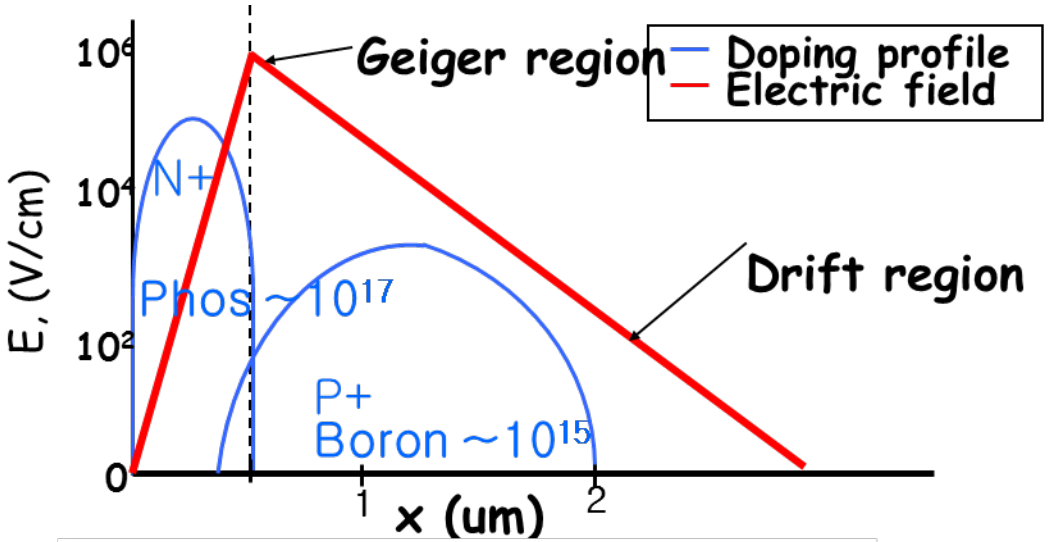
- **Development of SiPM and associated electronics**
  - Fabrication of SiPM (Poster)
  - Fabrication of Micron Resolution Optical Scanner (Poster)
    - R. A Shukla et.al, Review of Scientific Instruments 85, 023301 (2014)
  - Microscopic characterization of SiPM
  - Multichannel programmable power supply for SiPM (Poster)
    - R. A. Shukla etal. Review of Scientific Instruments 87, 015114,(2016)
  - High speed amplifiers and discriminators
  - General purpose DAQ Systems using USB, Ethernet etc. protocols

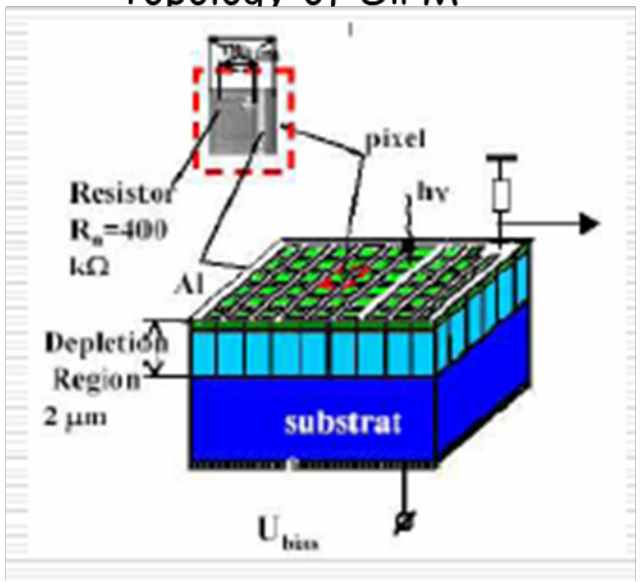
- **Application of these developments to various experimental activities and national needs**
  - Upgrade of HO Detector with SiPM
  - Design and Fabrication of HFRADMON system (Poster)
  - Replacing PMT Based scintillators with SiPM based scintillators for GRAPES-3
  - Microscopic characterization of SiPM for HB/HE/BH
  - Application of SiPM to VMS, ….

SiPM: Typical Design



Topology of SiPM





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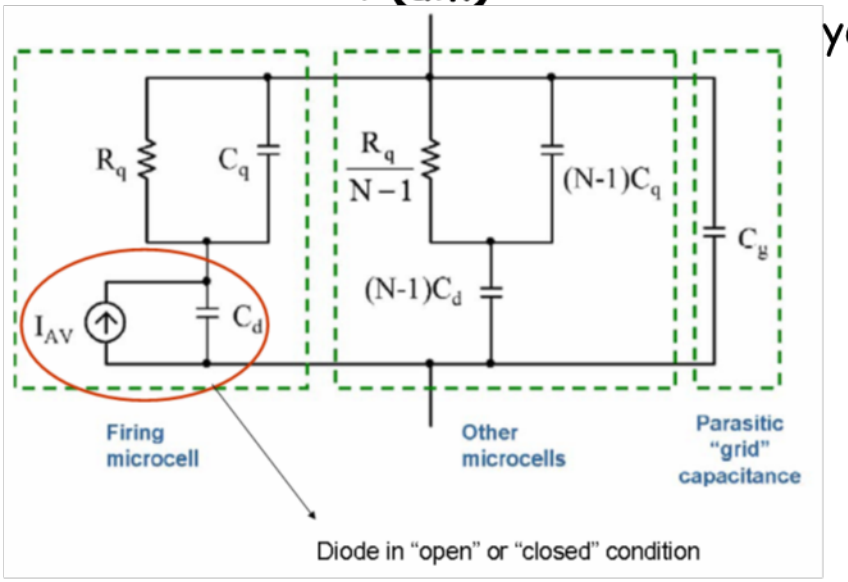
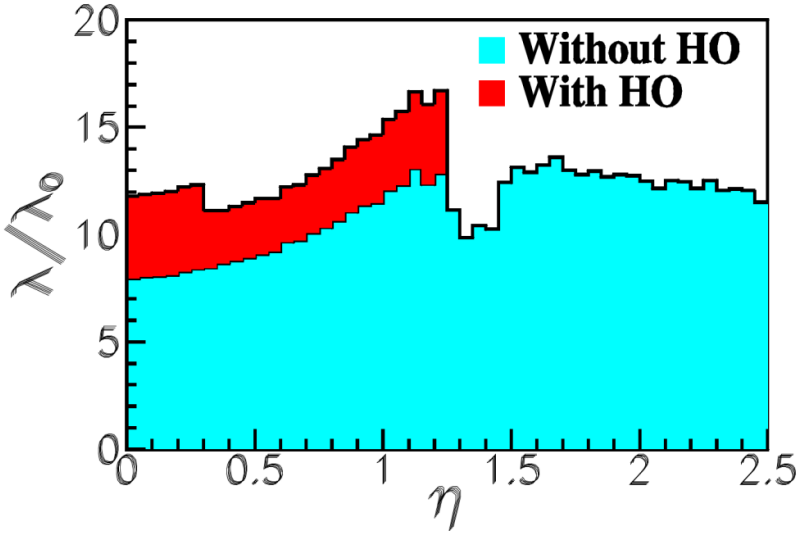
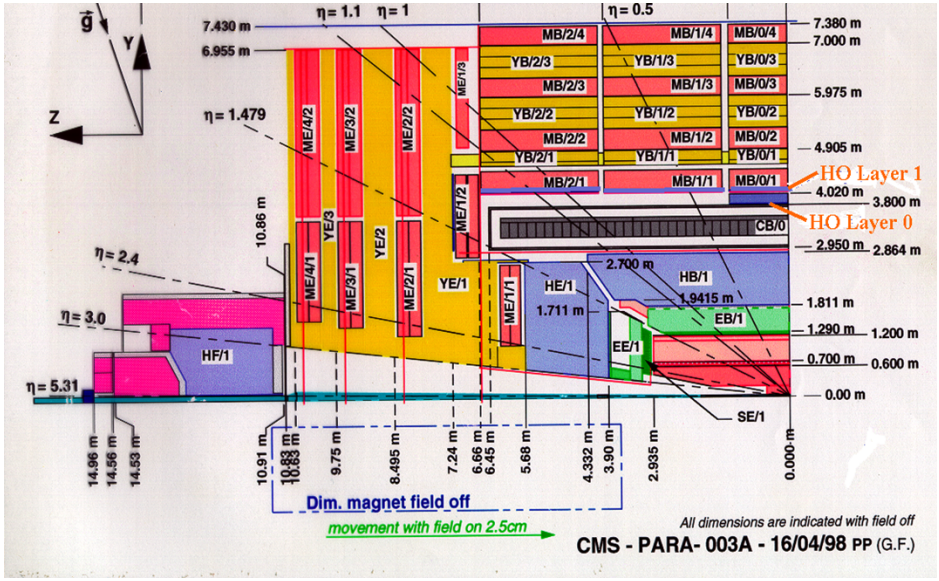
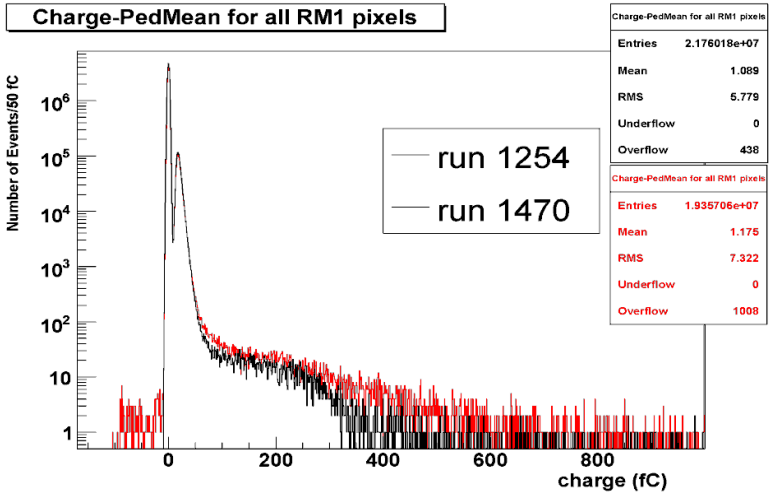


Outer Hadron Calorimeter (HO)

In the central region, HB is not thick enough to contain hadronic shower fully, particularly those fluctuated showers which develop deep inside the HCAL.



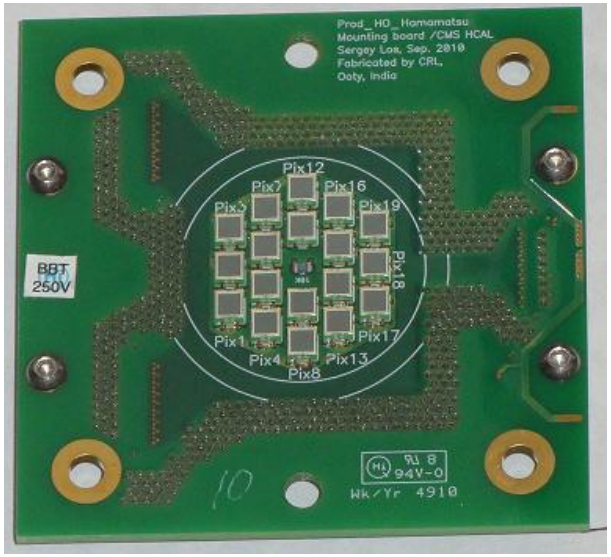




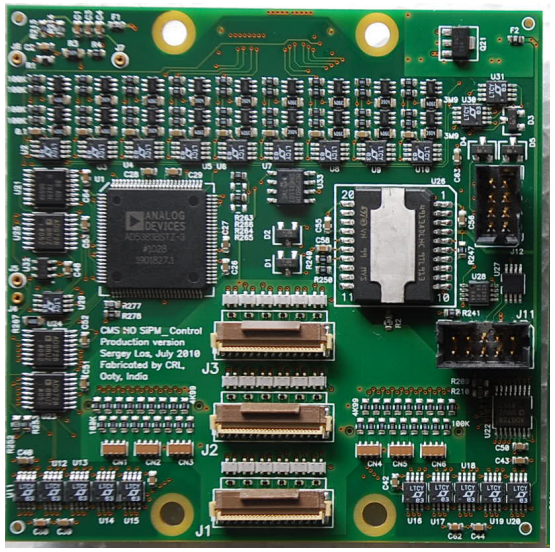
Scope of Activity

- Validation of SiPM for CMS environment
  - Testbeam studies, stability, radiation hardness, magnetic field immunity, saturation effects
- Fabrication of 160 SiPM Control Boards in India
  - Each board has 18 Channels
  - Control boards provides generates bias voltage for each channel, monitors current, temperature etc.
  - Entire production and quality control of 160 boards to be carried by Indian group in India
- Quality Control of Control Boards and SiPM Boards (160+160) at India:
  - Setting up stand-alone DAQ system for Control and SiPM boards
  - Development of software for QC Data Analysis
  - Generating QC report for each board
- Installation and Commissioning:
  - Removal of 132 Readout Modules, Assembly of Readout Modules, QC and burn-in test at CERN, Installation of 132 Readout Modules
- Project Leaders for Fabrication:
  - Jim Freeman (FNAL) and Shashi Dugad (TIFR)
  - *Funded by TIFR, FNAL, DESY*

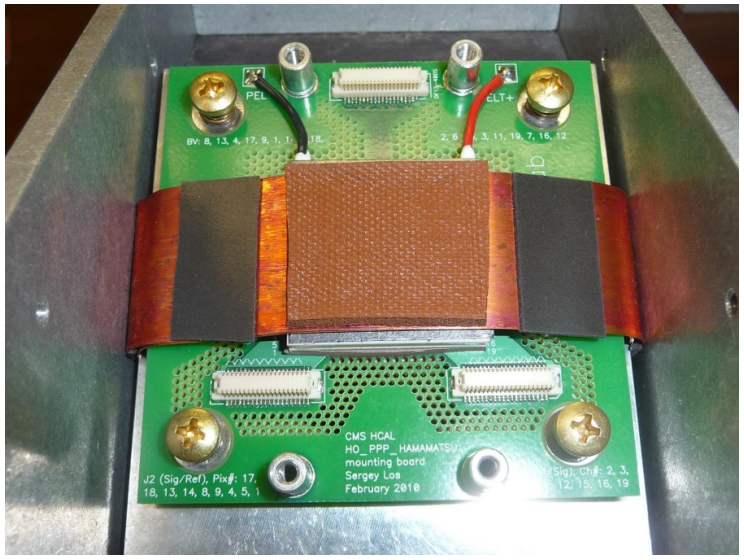
HO Readout Module Assembly

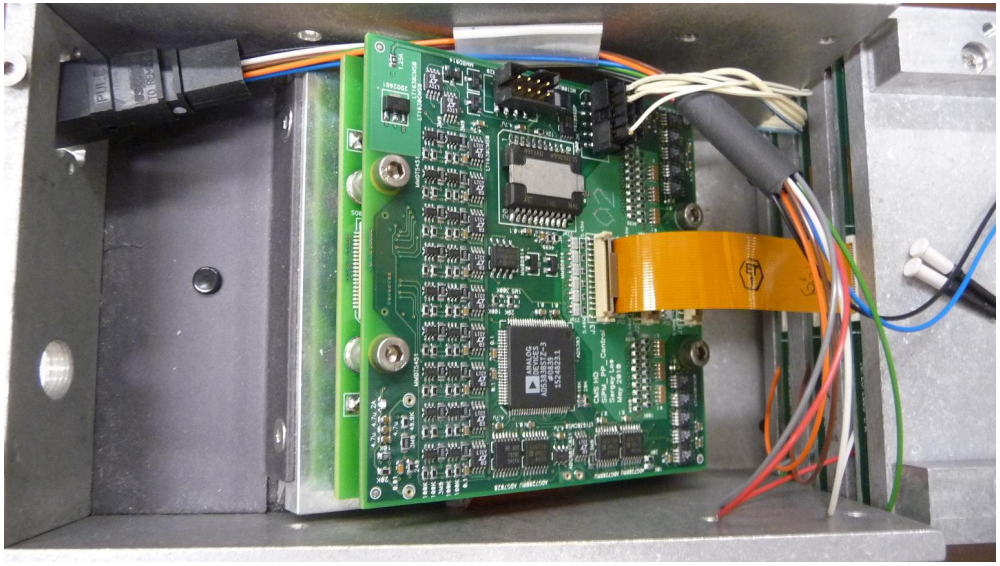


SiPM Mounting Board



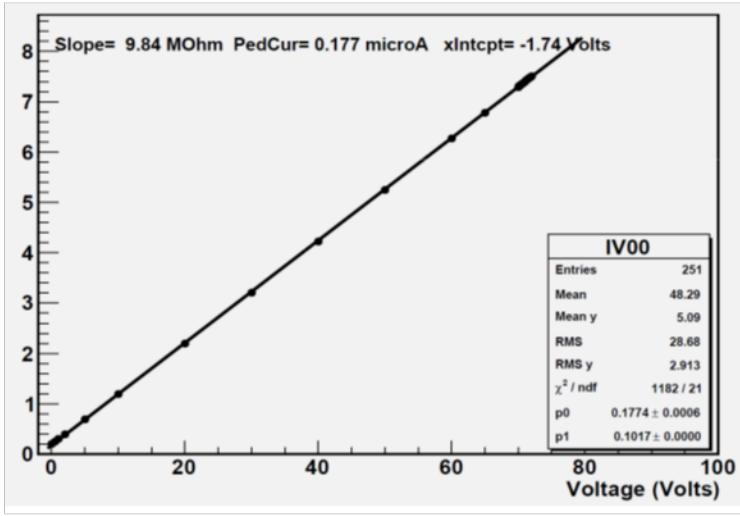
SiPM Control Board

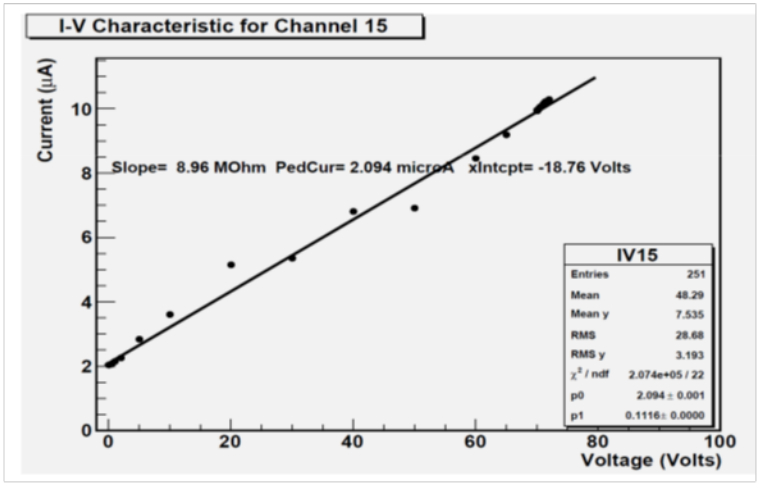


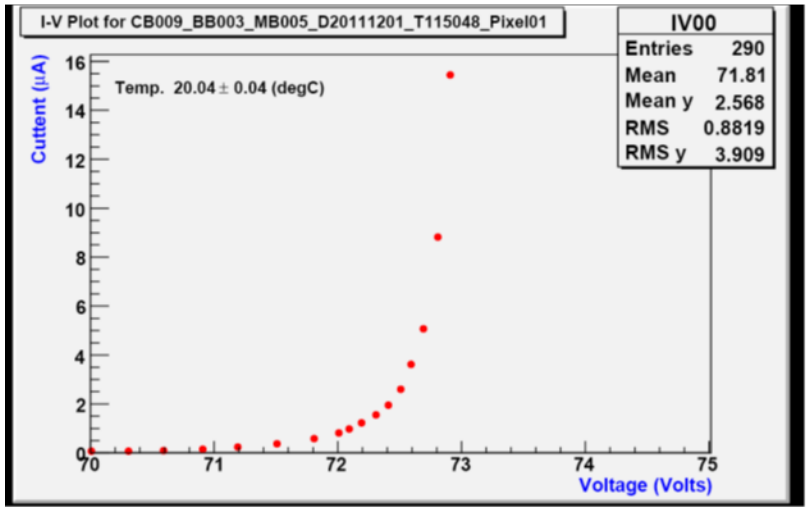


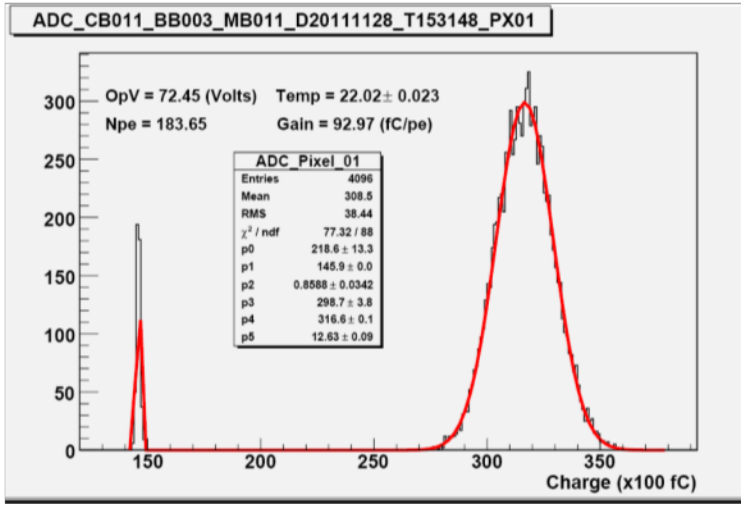
QC Results of HO Hardware

(Carried out at GRAPES-3, Ooty)

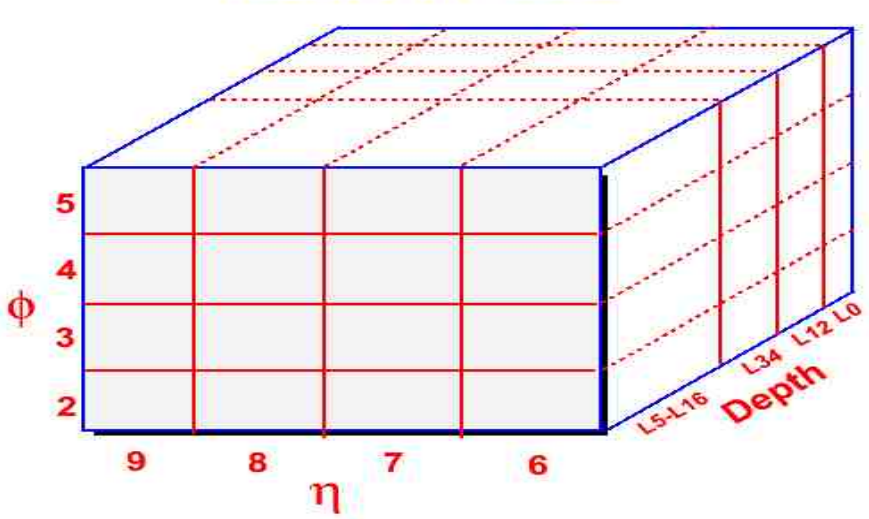


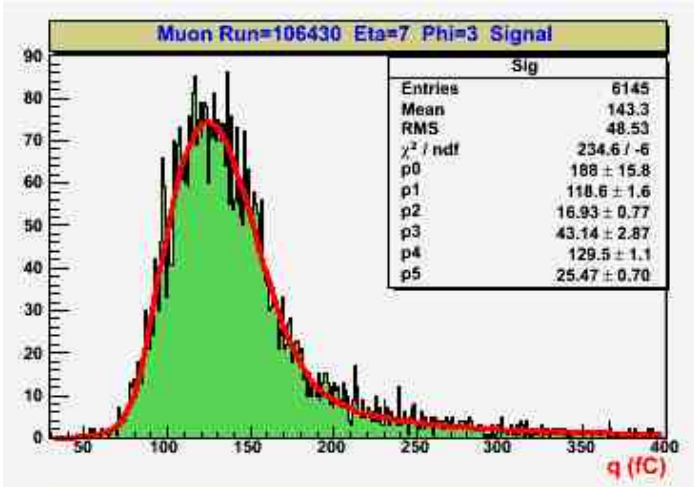


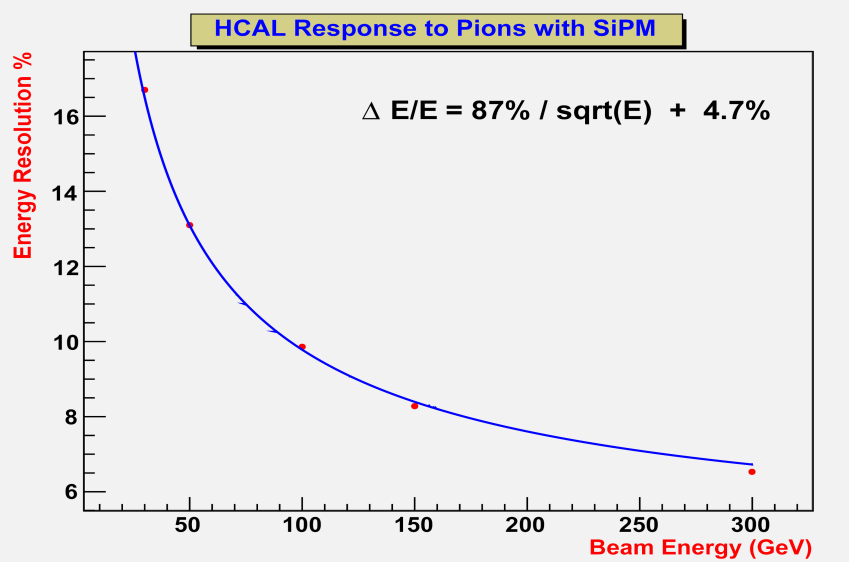


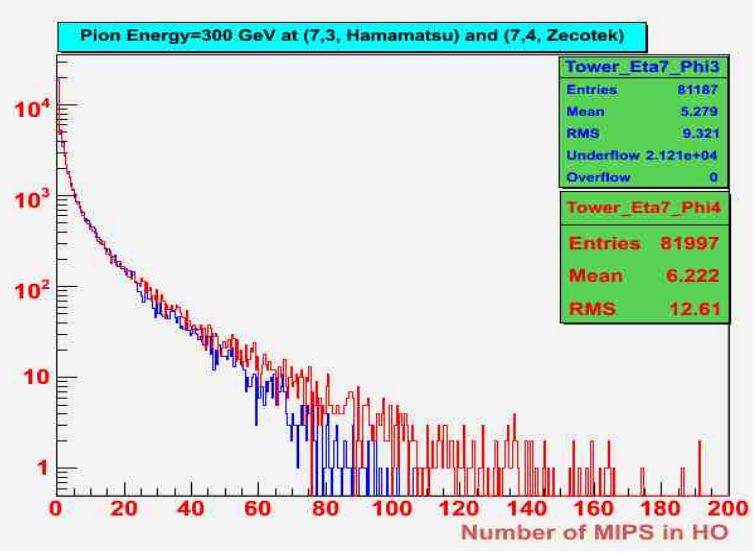


HO Response to muons, pions at Test-Beam

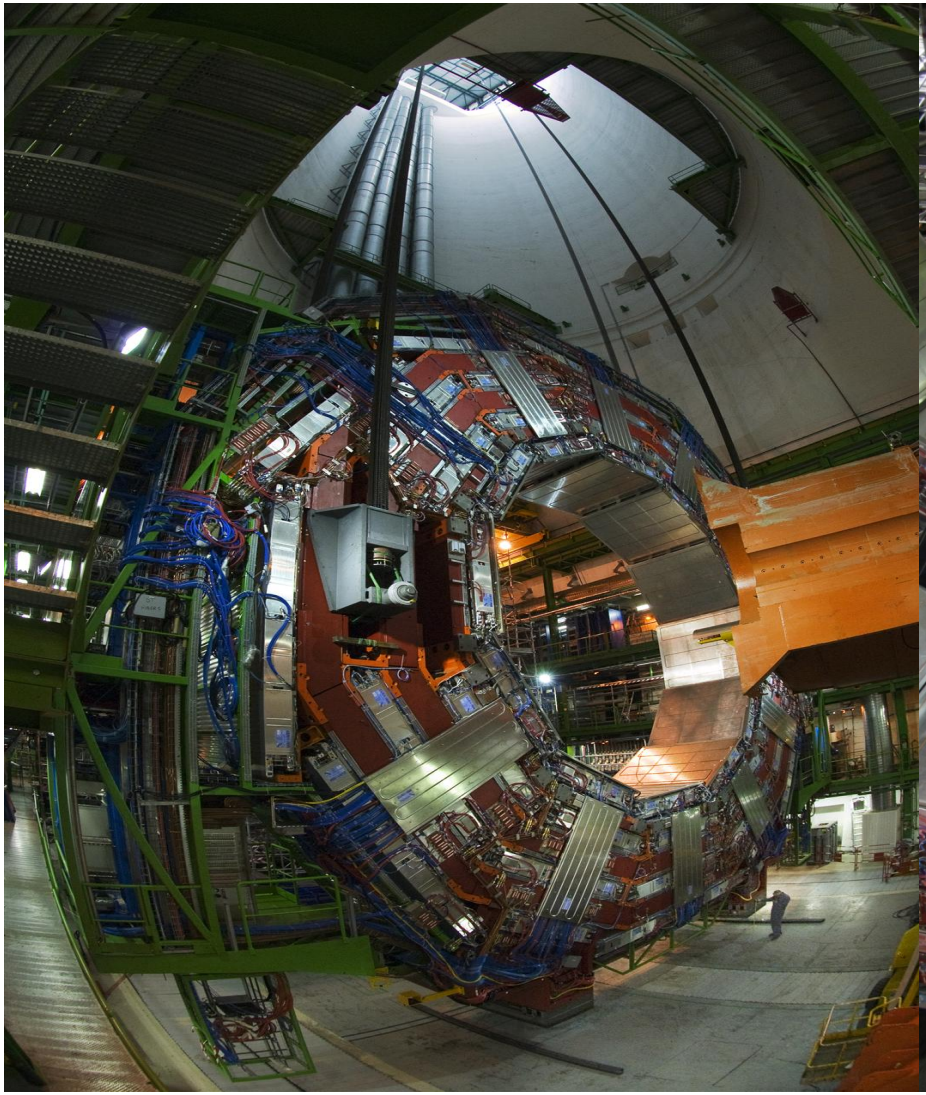


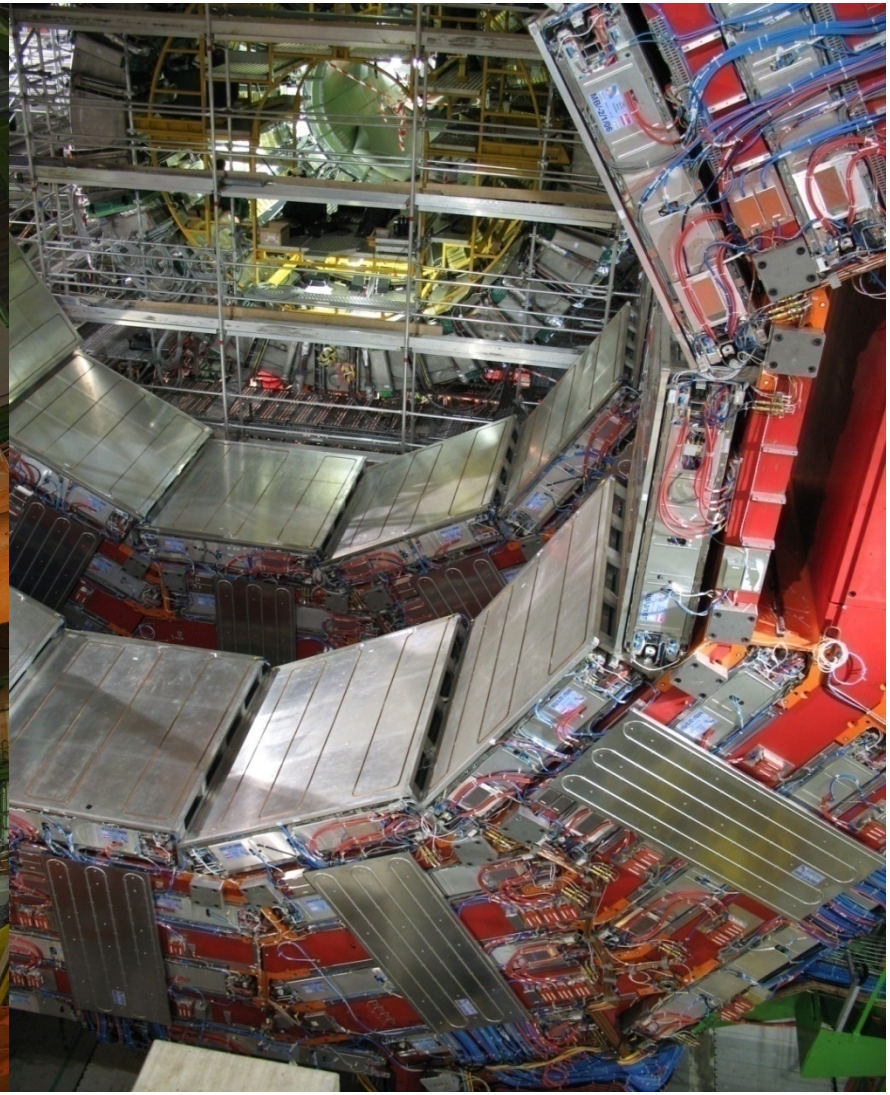






Outer Rings with instrumented HO





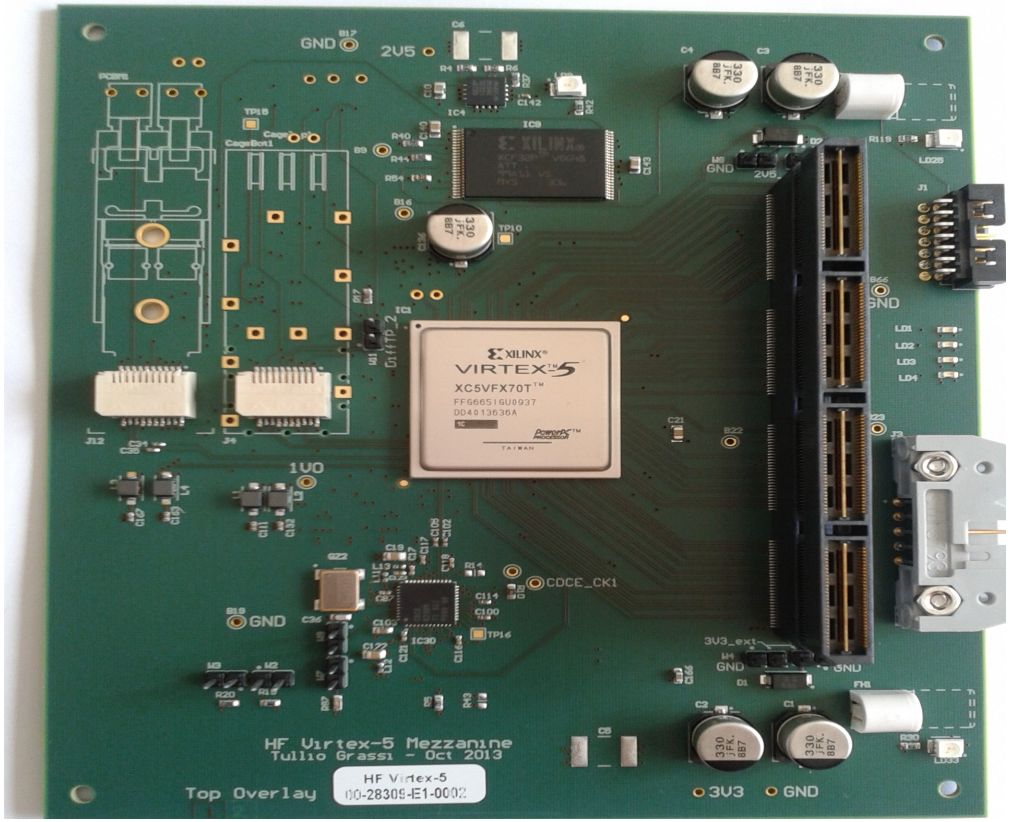
HO fully commissioned

Design Review of GBTX emulator FPGA board

- In the HCAL-CMS Group, a new GBTX emulator FPGA board to be used as a mezzanine card in the HF-ngCCM prototype was designed by Tullio Grassi.
- HCAL-CMS Group requested us to do a circuit design and PCB review of the same.

- The purpose of this review is to provide an independent assessment of the board design.
- The review ensured that all contributory factors and reasonable design options had been considered optimally and that the design met the requirements as outlined in the specifications by vendor for each component.

- Several recommendations and suggestions made during the review were incorporated into the final design. Detail Design Review Report is available on: https://cms-docdb.cern.ch/cgi-bin/PublicDocDB//ShowDocument?docid=11876

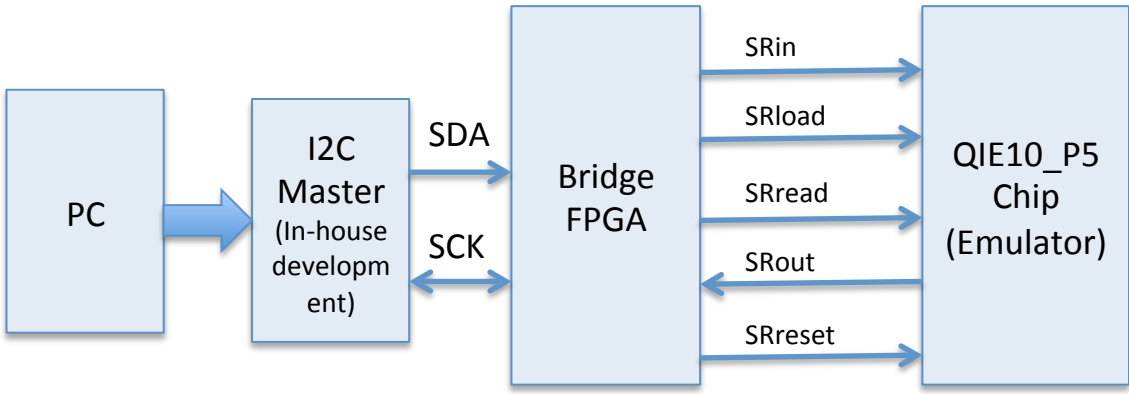


PCB GBTx emulator mezzanine card

Firmware Development for Front End Electronics Configuration (QIE-10)

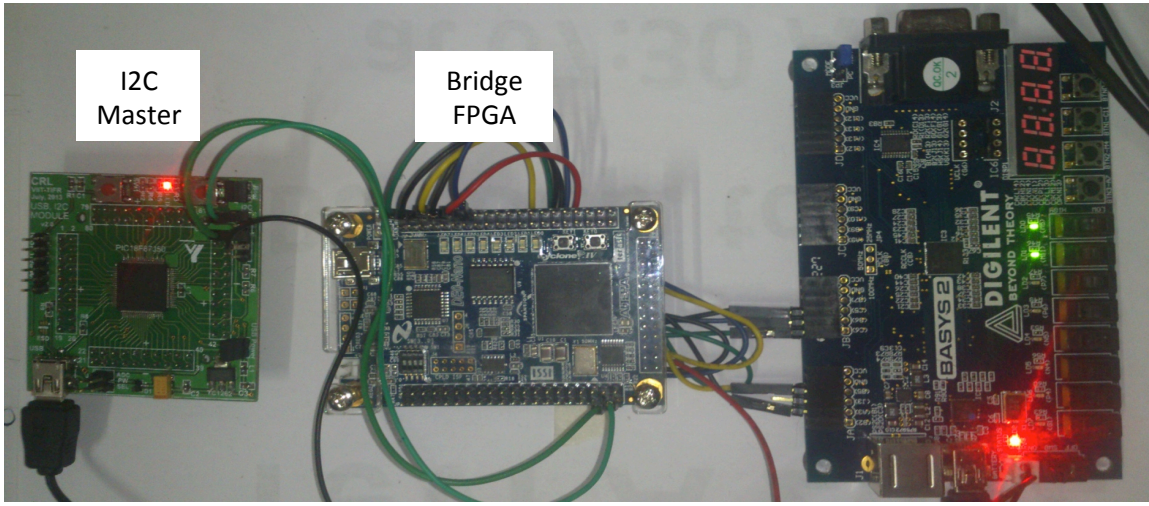
- QIE10 chips are designed at CERN for integrating fast electronic pulses coming from detectors.
- Thus, QIE10 chip forms a important building block of the Front-End electronics.

- QIE10 chips have programmable parameters and thus appropriate parameters needs to be programmed into the chip for required operation

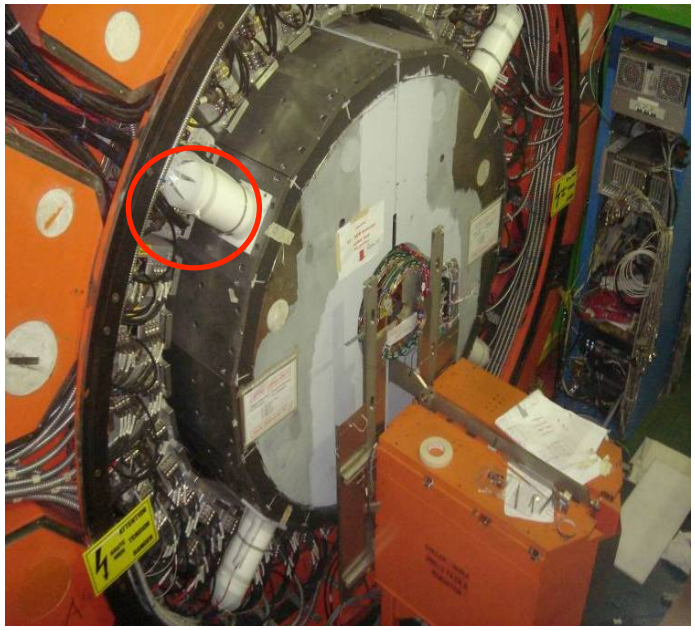


- A FPGA is responsible for programming (~24) QIE10 chips on a board
- Thus FPGA plays a crucial role of a bridge between upstream controller and a downstream QIE10 chip.
- FPGA acquires the programming parameters (64 bit for each chip) via I2C bus and programs them into the QIE10 chip via custom serial protocol.

QIE10_P5 Chip (Emulator)



HF Radiation Monitors



Objective of the monitors:

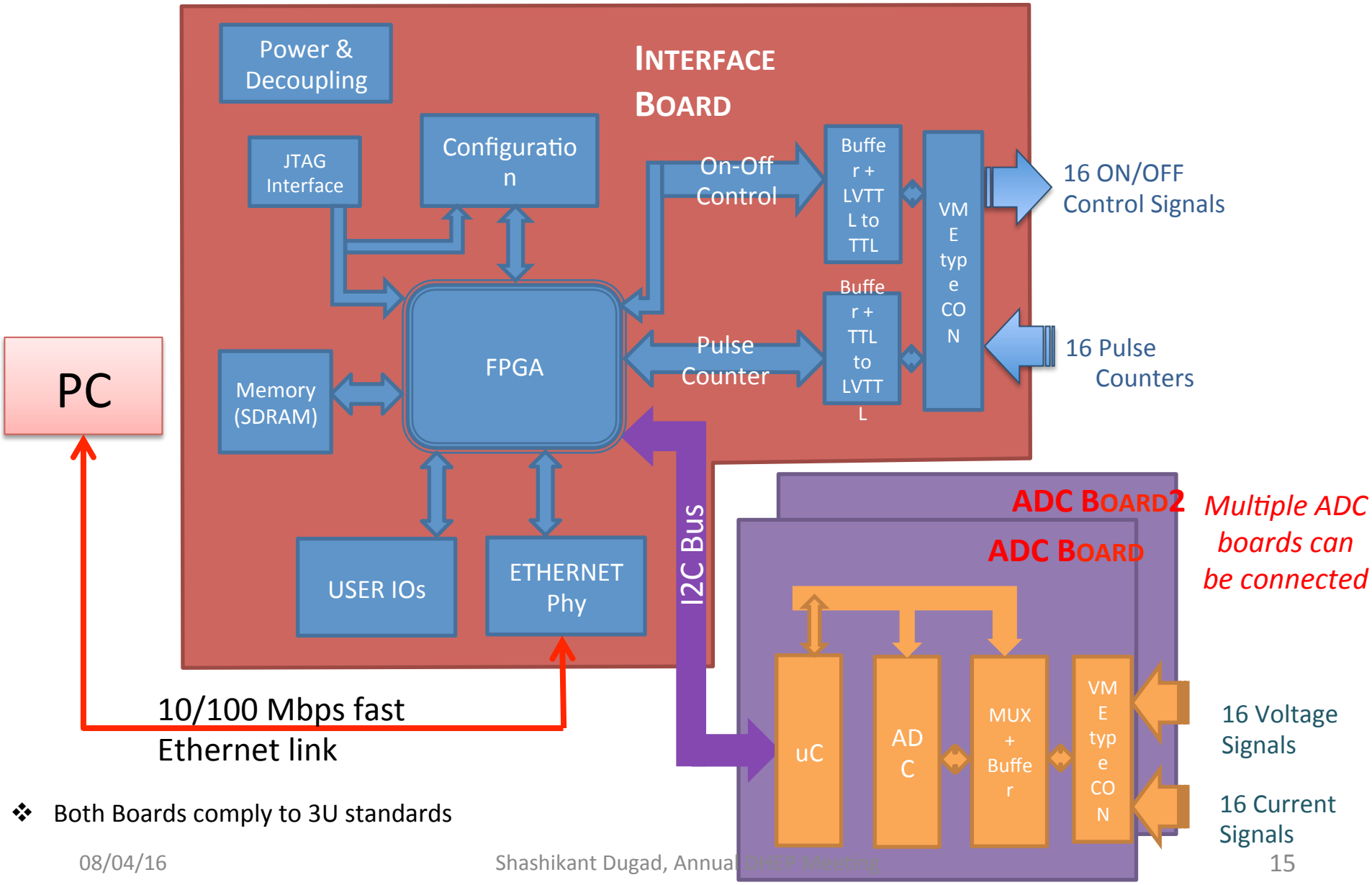
- ✓ **Long term monitoring of the absorbed dose and neutron flux to estimate the expected degradation of fibers, electronics, PMTs and to measure the shielding efficiency.**
- ✓ **Additional monitoring of the HF itself performance for future re-calibration etc.**

- Control and Monitoring of 16 channels (detectors):
  - Control ON/OFF signaling (TTL)
  - 32-bit count of asynchronous pulses (TTL), rate 1MHz
  - Voltage and Current Monitoring (Range: 0-10V)
- Readout: 10 Hz with Ethernet

➢ Old system was monitored through ***NI-DAQ cards*** with PCI interface.

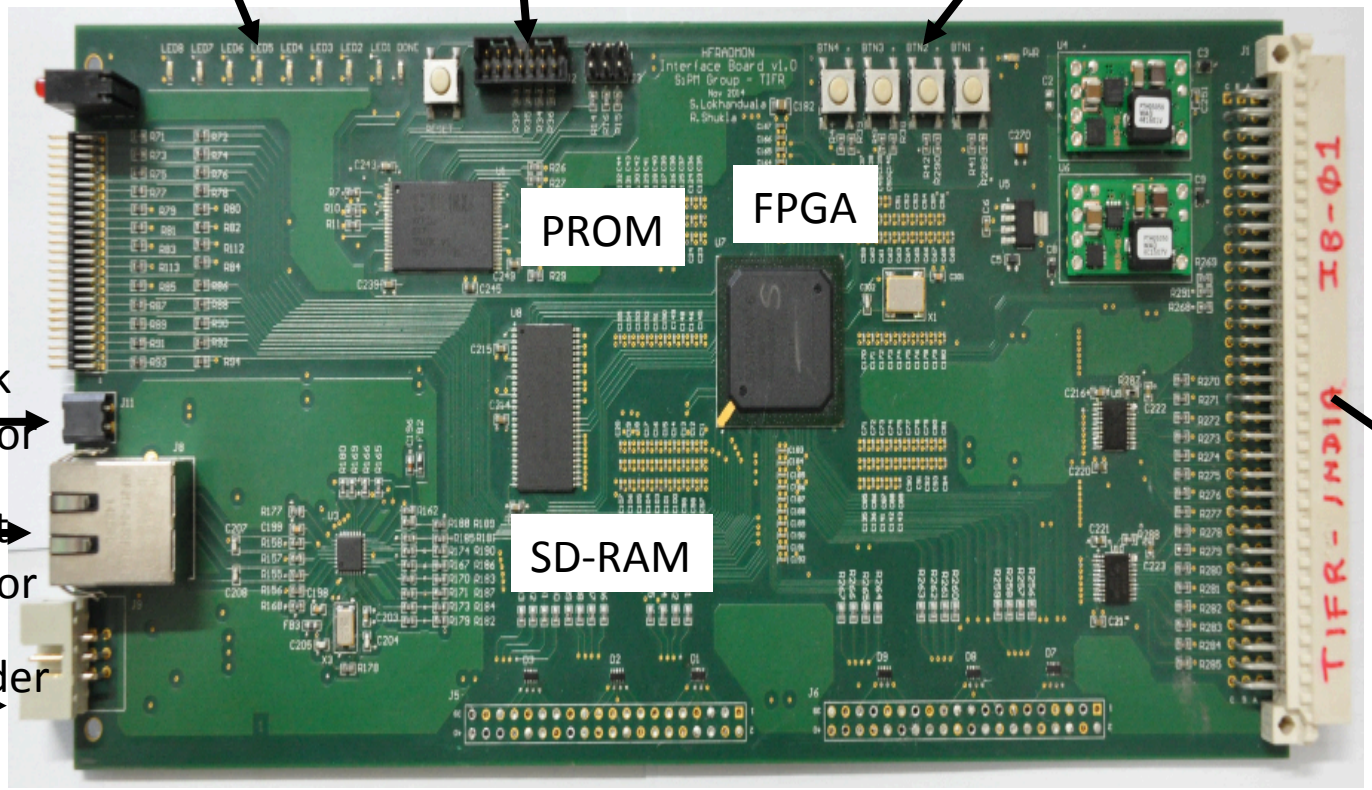
➢ PCI is phased out at CMS (moreover, NI cards are 5V PCI) and drivers are only 32bits.

Block Diagram of New DAQ

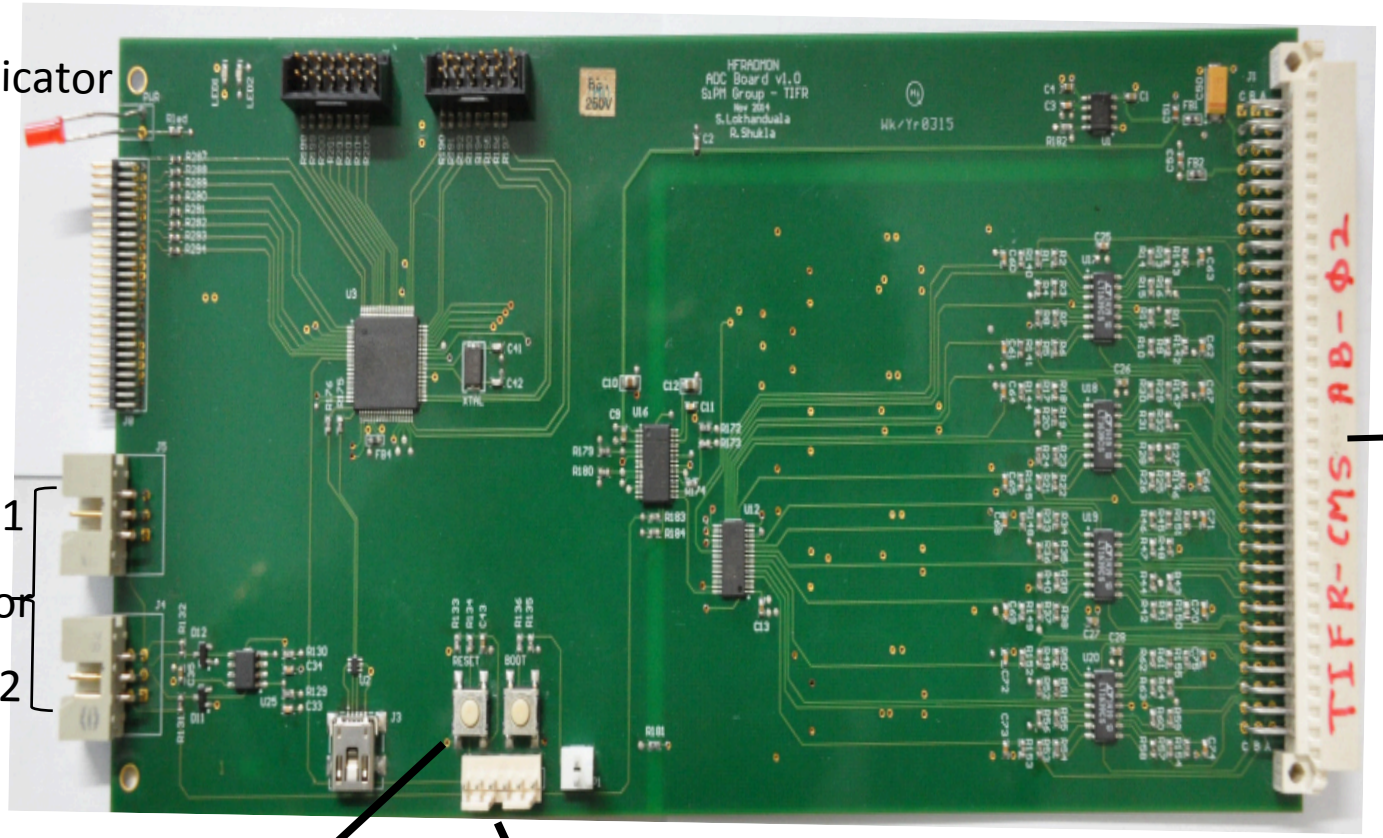


- Both Boards comply to 3U standards

Interface board



ADC board


Power Indicator LED
1
I2C Connector
2
Backplane connector
Reset switch
ICSP Programming header
HFRADMON
ADC Board v1.0
S.Lokhandwala
R.Shukla
TIFR-CMS AB-Φ2

Interface board features and specification

Interface board is controlled by powerful Xilinx Spartan-6 FPGA

- 10/100 Mbps fast Ethernet link
- I^2C Master controller for ADC board data acquisition
- 16, 32-bit high speed counters with TTL inputs
- 16-ch detector on/off control with TTL logic
- Interlock logic, ms time stamp clock
- Onboard status monitoring logic
- Onboard 16 Mbit flash PROM for permanent program storage
- Buffers and ESD protection for outside input/outputs
- 32 MB RAM for future use

ADC board is controlled by *PIC-µController*

- I^2C interface for readout and configuration
- All channels are sampled in one cycle with high speed ADC
- Over/Under flow indication with programmable threshold (0-10 V)
- **Samples:**
  - 32 Detector differential analog signals (voltage and current).
  - 3 analog temperature sensors
  - All on board voltage buses
- Multiple ADC board can be connected on the I^2C bus
- A stand-alone system; can be accessed from any I^2C master : simple and elegant

Interface and ADC board Firmware

Firmware for Spartan-6 FPGA

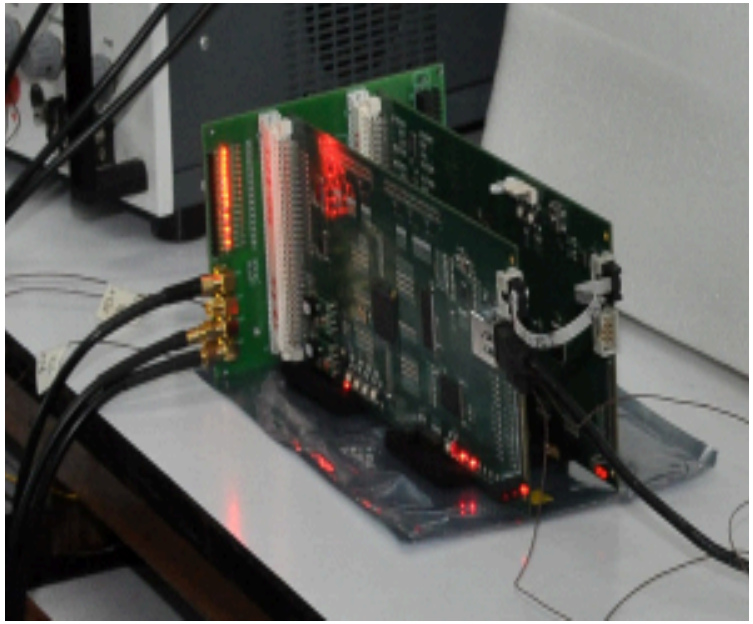
- ✓ Complete code written in Verilog
- ✓ In-house development of UDP soft-IP core
- ✓ 16, 32-bit high speed async counters
- ✓ Two internal counters for precise calibration of time-base
- ✓ I^2C Master controller for ADC board readout
- ✓ 32-bit checksum generation to check data integrity
- ✓ Internal and External Interlock Logic (Emergency stop)
- ✓ Detector status display with online fault monitoring logic
- ✓ Timestamp with 1ms 48-bit free running counter

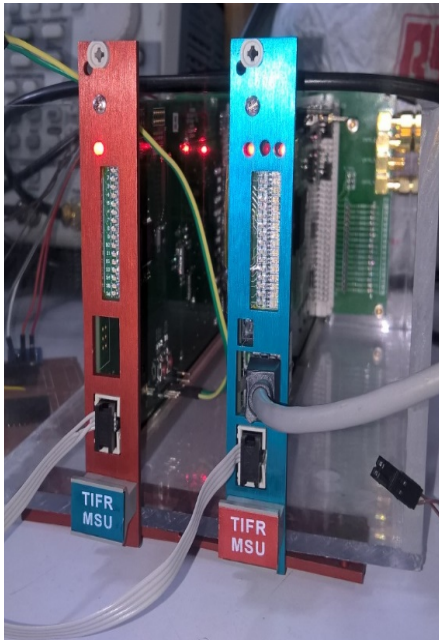
Firmware for PIC Microcontroller

- ✓ Firmware has been written in embedded C
- ✓ Microcontroller acts as I^2C master as well as slave; controls on-board peripherals as a I^2C Master and responds to data read query from Interface board as I^2C slave
- ✓ The I^2C address of slave is programmed in firmware and can be any 7-bit number
- ✓ This allows for connecting many ADC boards together on common I^2C bus
- ✓ All analog channels (16 V, 16 I, temperature etc) sampled at programmable interval
- ✓ Online detector health monitoring and LED display
- ✓ 16-bit sampling event counter

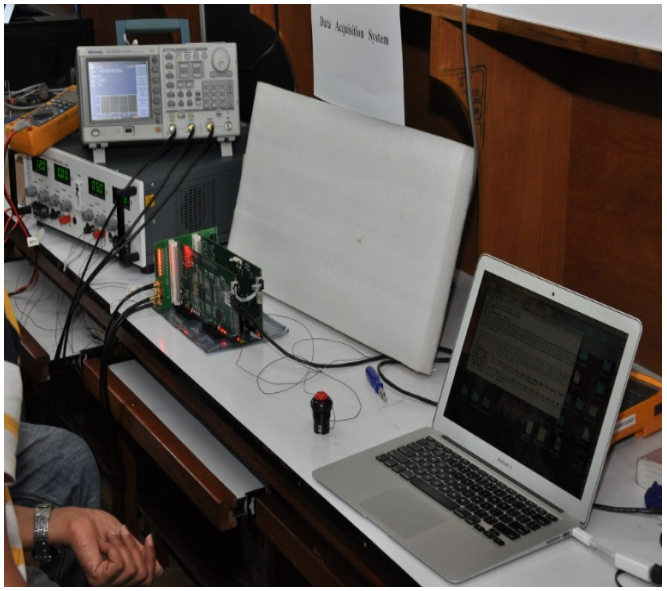
Testing @ TIFR

- Rigorous QC tests before and after assembly
- Test jigs made at TIFR for testing various functionalities
- Development of PC side code for configuration, status monitoring and data acquisition
- Detailed analysis program developed with ROOT framework
- Long term stability tests carried out for more than 8 days

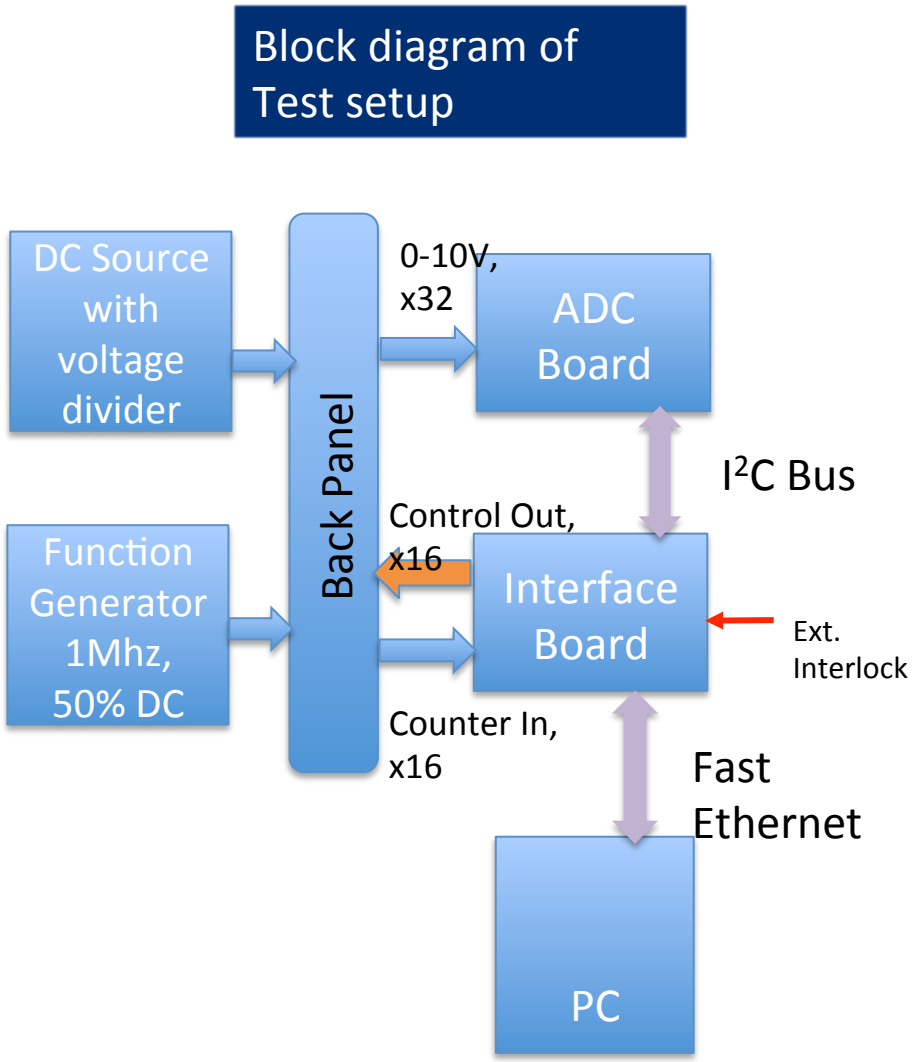




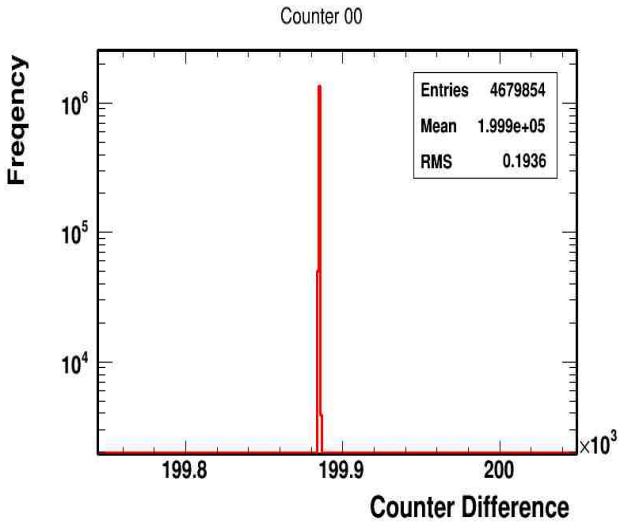
Test Setup

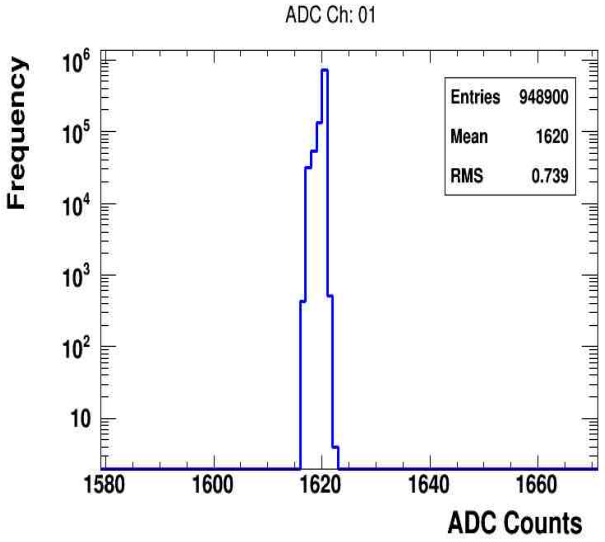


- ✓ Data from interface board is requested at every 60 ms
- ✓ All the data including counters, ADC counts and status information is logged into a file
- ✓ Data file analyzed off-line with ROOT utility

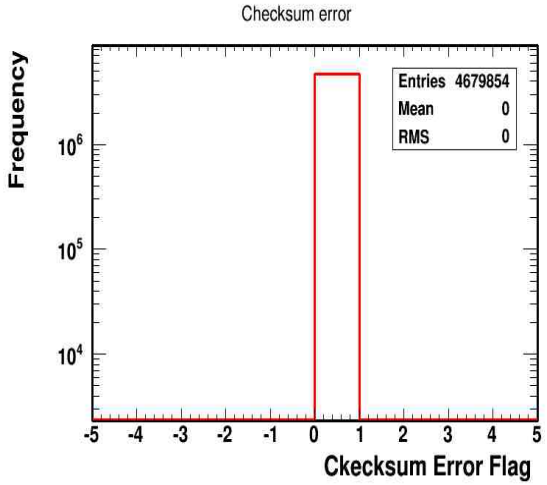


Test data analysis

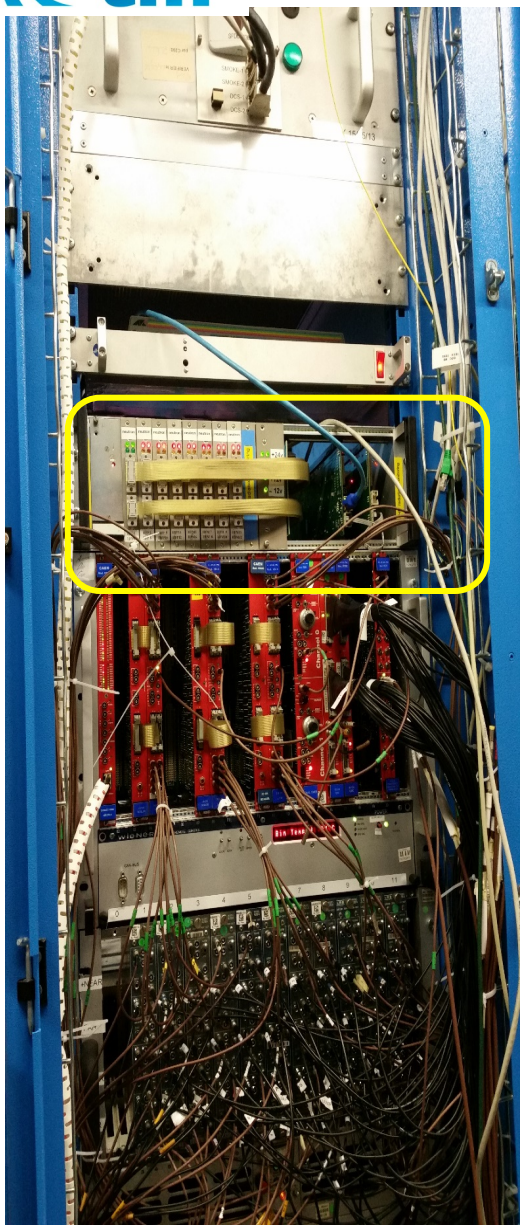




- Counters are free flowing and accumulates the counts asynchronously
- The difference between successive latch values is plotted
- No checksum error has been detected: High data integrity



Commissioning at CERN

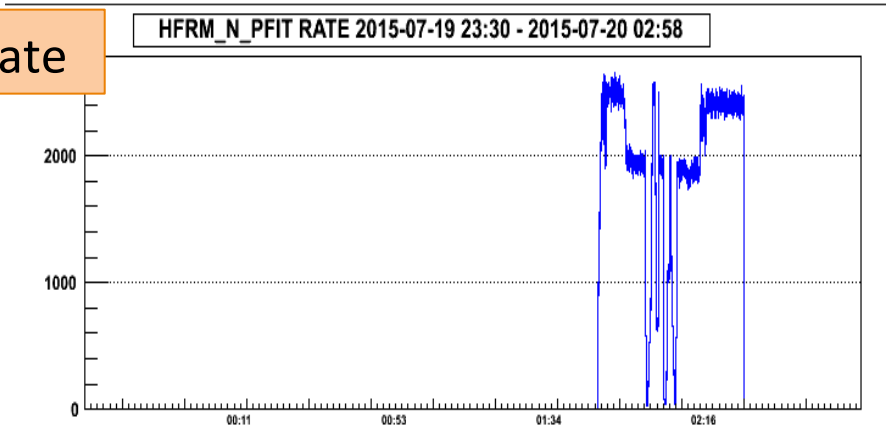


- The hardware has been successfully installed at P5 at CERN
- No issues reported so far
- Data is published online for debugging and monitoring purpose
- Public web page can be seen at :

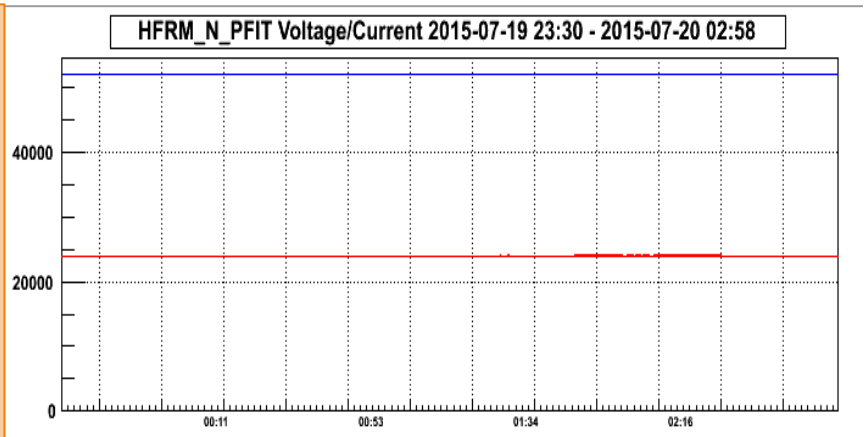
  http://odin.sinp.msu.ru/rmpeek/index.py

Plots from online monitoring utility

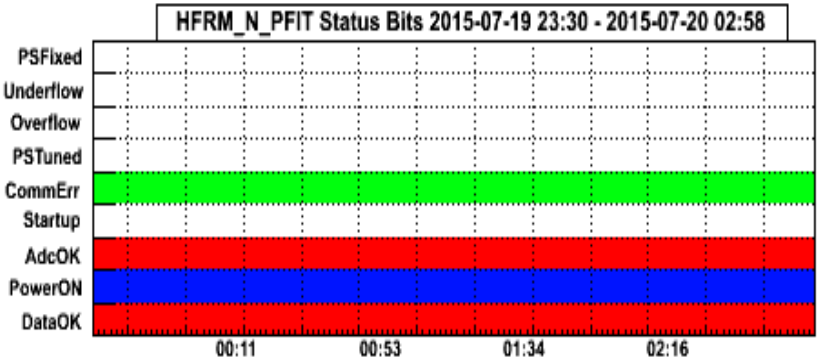
Rate



Voltage and Current



Status bits



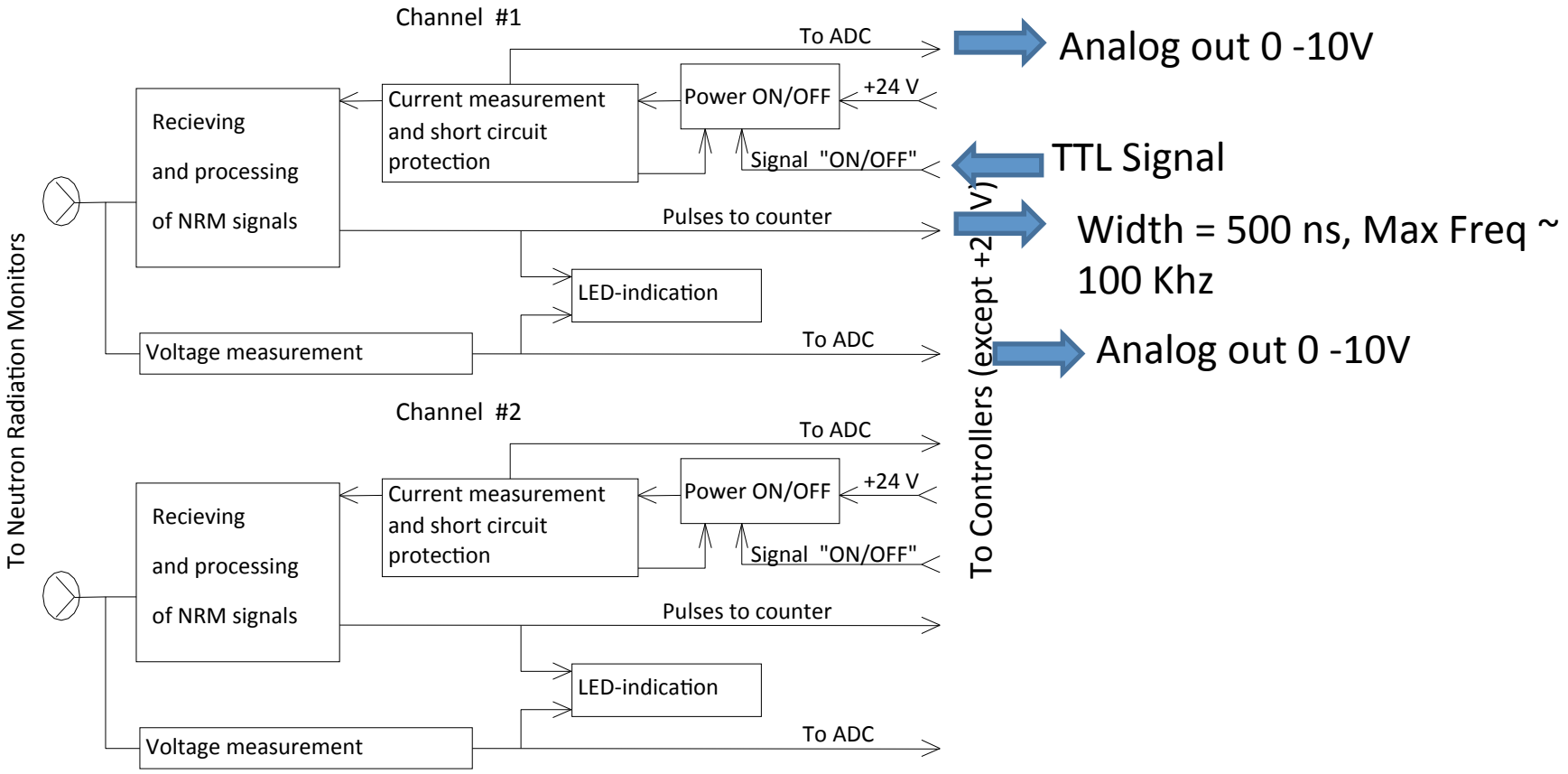
To peek at latest data and status:
http://odin.sinp.msu.ru/rmpeek/index.py

Start and End time can be picked up from:
https://cmswbm.web.cern.ch/cmswbm/cmsdb/s

Summary

- **Collaboration with HCAL CMS has significantly strengthen our in-in-house developmental activities**
- **A complete vertical slice for using SiPM with associated front end electronics and slow control system has been developed in our laboratory**
- **Unique characterization facilities for photo devices**
- **Major hardware upgrade tasks for CMS completed successfully**
- **Looking forward to utilize in-house expertise for CMS upgrade, GRAPES-3 scintillator readout upgrade and national needs**

HF Radiation Monitors – Old Electronics



Schematic of the NRM adapter