Electronics, trigger and data acquisition systems for the INO ICAL experiment

B.Satyanarayana

For and on behalf of the INO/ICAL Electronics team

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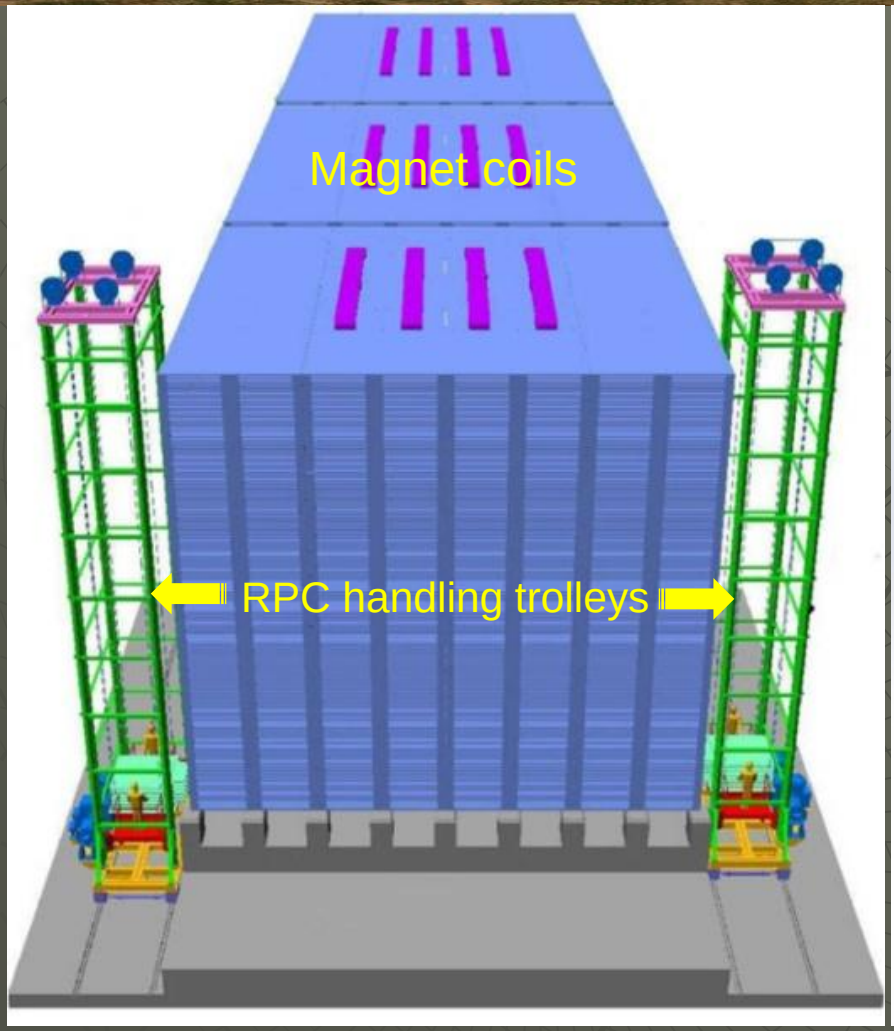
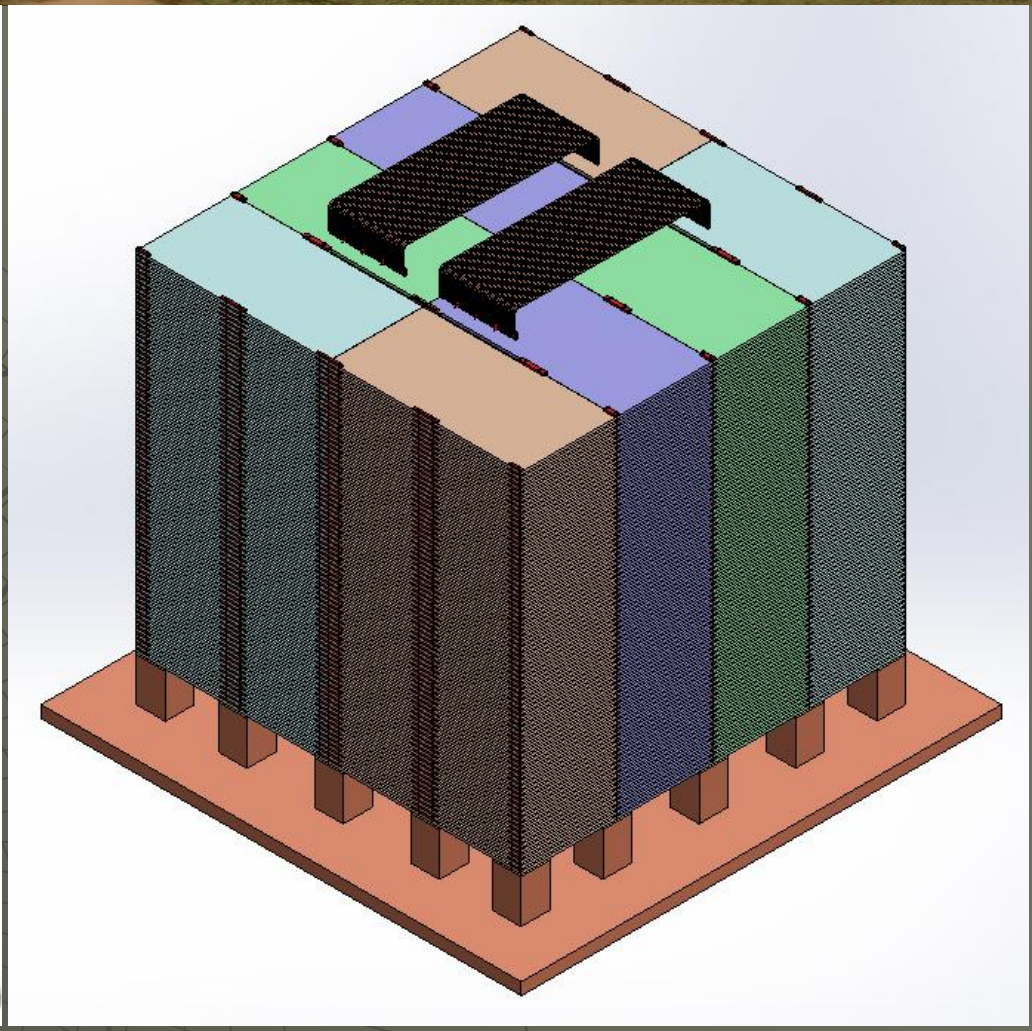
Please visit posters for details

- Analog Front End Solutions for ICAL RPCs
- Front End Data Acquisition and Control Module for ICAL RPCs
- Global Services and Calibration for the INO ICAL Electronics
- Multilevel and Configurable Trigger System for INO-ICAL Experiment
- INO-ICAL: Network Scheme for Distributed Data Processing

ICAL and its Engineering Module





Some facts and figures

Parameter	ICAL	ICAL-EM
No. of modules	3	1
Module dimensions	16.2m × 16m × 14.5m	8m × 8m x 2m
Detector dimensions	49m × 16m × 14.5m	8m × 8m x 2m (89:1)
No. of layers	150	20
Iron plate thickness	56mm	56mm
Gap for RPC trays	40mm	40mm
Magnetic field	1.3Tesla	1.3Tesla
RPC dimensions	1,950mm × 1,910mm × 24mm	1,950mm × 1,910mm × 24mm
Readout strip pitch	3 0mm	3 0mm
No. of RPCs/Road/Layer	8	4
No. of Roads/Layer/Module	8	4
No. of RPC units/Layer	192	16
No. of RPC units	28,800 (107,266m^2)	320 (1,192m^2) (90:1)
No. of readout strips	3,686,400	40,960 (90:1)

Challenges of ICAL electronics

- Large number of electronic data readout channels. This necessitates large scale integration and/or multiplexing of electronics.
- Large dimensions of one unit of RPC. This has bearing on the way the signals from the detector are routed to the front-end electronic units.
- Large dimensions of the ICAL detector. Disparate distances (i.e. delays of signals in cables) of RPCs from the backend requires elaborate calibration procedures for global signals.
- Road structure for the mounting of RPCs. This necessarily imposes constraint that signals from both X & Y planes of the RPC unit, along with other service and power supply lines are brought out only from the transverse direction of the detector.
- About 25cm gap is available between the face of the detector and the service trolleys. Any installations on the face of the detector have to be designed with this consideration.
- About 40mm gap between iron layers is available for the RPC detector. Thickness of the RPC holding tray, thickness of tray sliding track, tolerances of the iron plate thickness, height of the on detector high voltage module, analog and digital front-end modules, routing of cables and all other service lines must fit in this gap.
- Effect of fringe magnetic field on the performance.
- Low power consumption per channel (25mW/channel $\rightarrow$ 100KW/detector)
- Long service life of electronics, component spares availability/replaceability is major a concern.

Design inputs to electronics

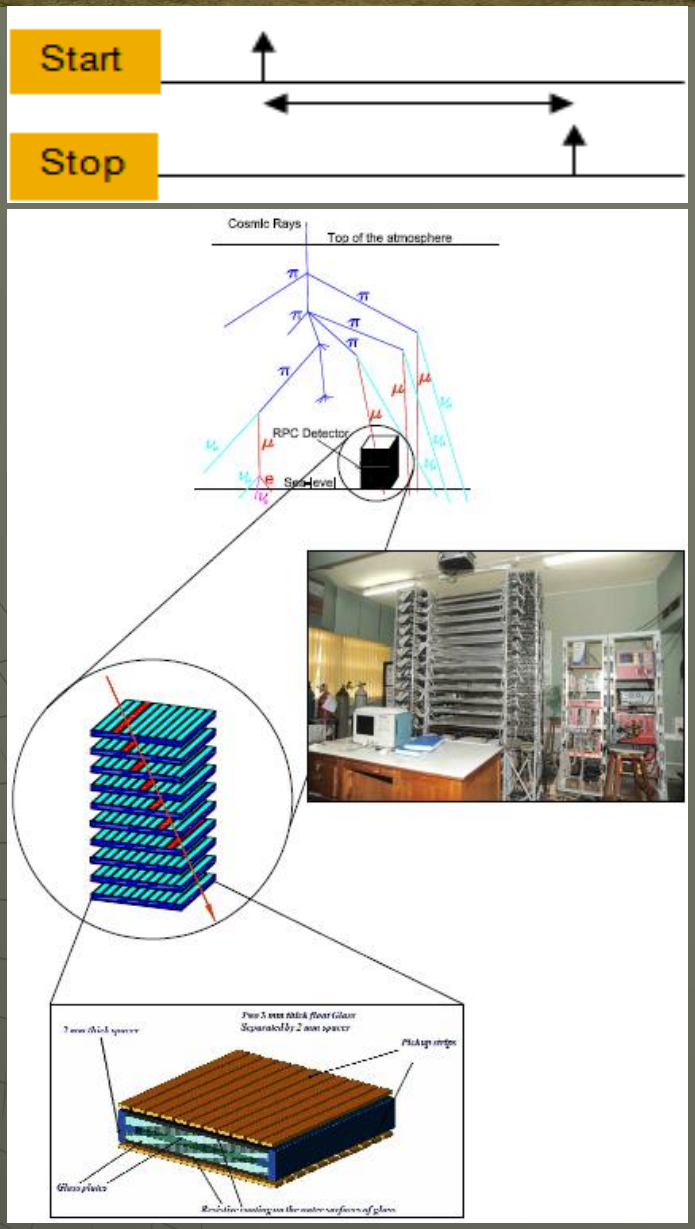
- RPC strip's characteristic impedance: 50±3Ω. Strip capacitance (1m): ~60pF. Signal coupling: DC
- RPC signal's rise time is of the order of 500-800ps. Therefore, we will need a resolution of about 200ps for the timing devices used for recording RPC signal arrival times w.r.t to ICAL trigger.
- The opening width of the amplified signals is of the order of 25nSecs. The minimum width of the RPC pulse over the threshold in the avalanche mode is as low as a few ns. This is an important input for the front-end electronics design.
- Mean strip pulse amplitude: ~0.6pC. The amplifier in the avalanche mode preferably should have a fixed gain in the range 100-200 depending on the noise levels obtainable and hence the minimum discriminator levels settable.
- Discriminator overhead (ratio of average peak pulse height to discriminator level) of 3-4 is preferable for reliable performance. Variable (but common) threshold in the range of ±10 to ±50mV for the discriminators should be supported.
- Timing measurement: 200ps (LC), multi-hit, both edges

RPC strip rate considerations

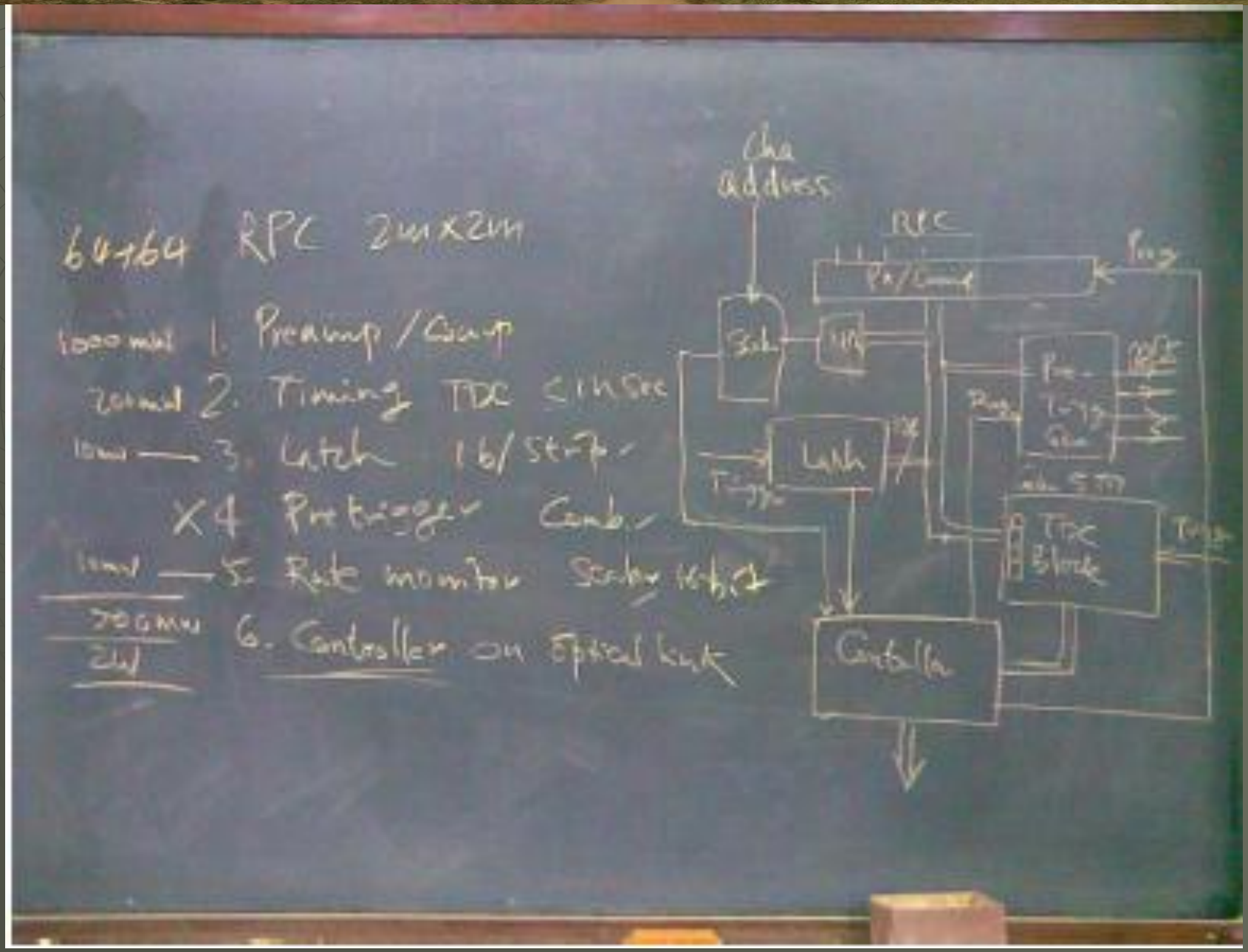
- RPC strip signal rates mainly contributed by the surrounding low energy activities such as stray radioactivity, local electrical discharges, dark currents of the detector and other electrical/electronic disturbances.
- For a given RPC, installed at particular location, operating at a particular high voltage, and a gas mixture, the average counting rate or *noise rate* is fairly constant and is in fact commonly used to monitor the stability of the above mentioned RPC operating parameters.
- One of the main background tasks (while not collecting event data) of the ICAL DAQ system is to sequentially monitor individual strip rates of all the RPCs in the detector, with a reasonable (of the order of 1 hour cycle time for a strip) frequency.
- Average RPC strip rate is ~200Hz (on surface).
- The noise rate has consequences on the design of trigger system. The threshold of the trigger system is such that it shouldn't generate triggers due to chance coincidence of noise rates.
- Event rate is ~10Hz (nominal)

Functions of ICAL electronics

- Signal pickup and analog front-end
- Strip hit latch
- Pulse shapers, timing units
- Background noise rate monitor
- Digital front-end and controller
- Data network interface and architecture
- Multilevel trigger system
- Backend data concentrators
- Event building, data storage systems
- On-line data quality monitors
- Slow control and monitoring
  - Gas, magnet, power supplies
  - Ambient parameters
  - Safety and interlocks
- Voice and video communications
- Remote access to detector sub-systems and data

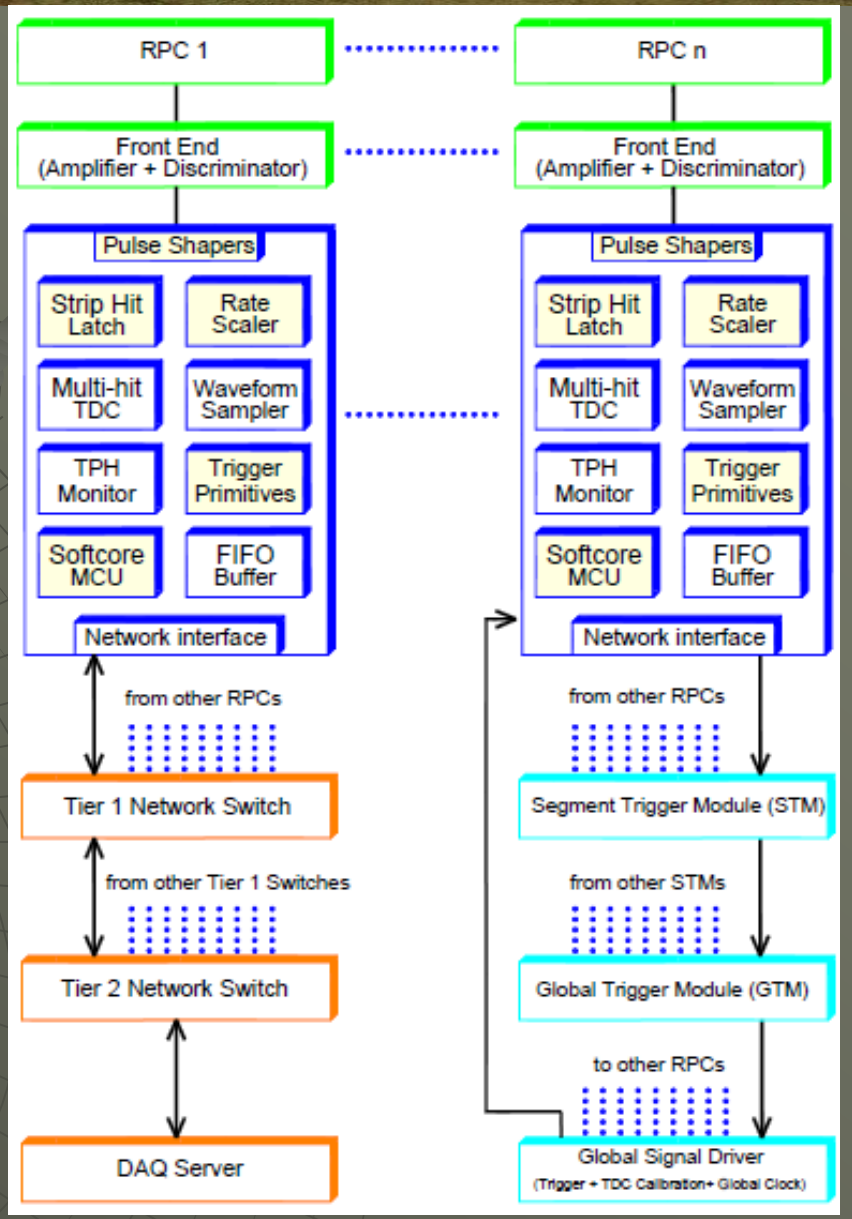


First sketch of ICAL electronics

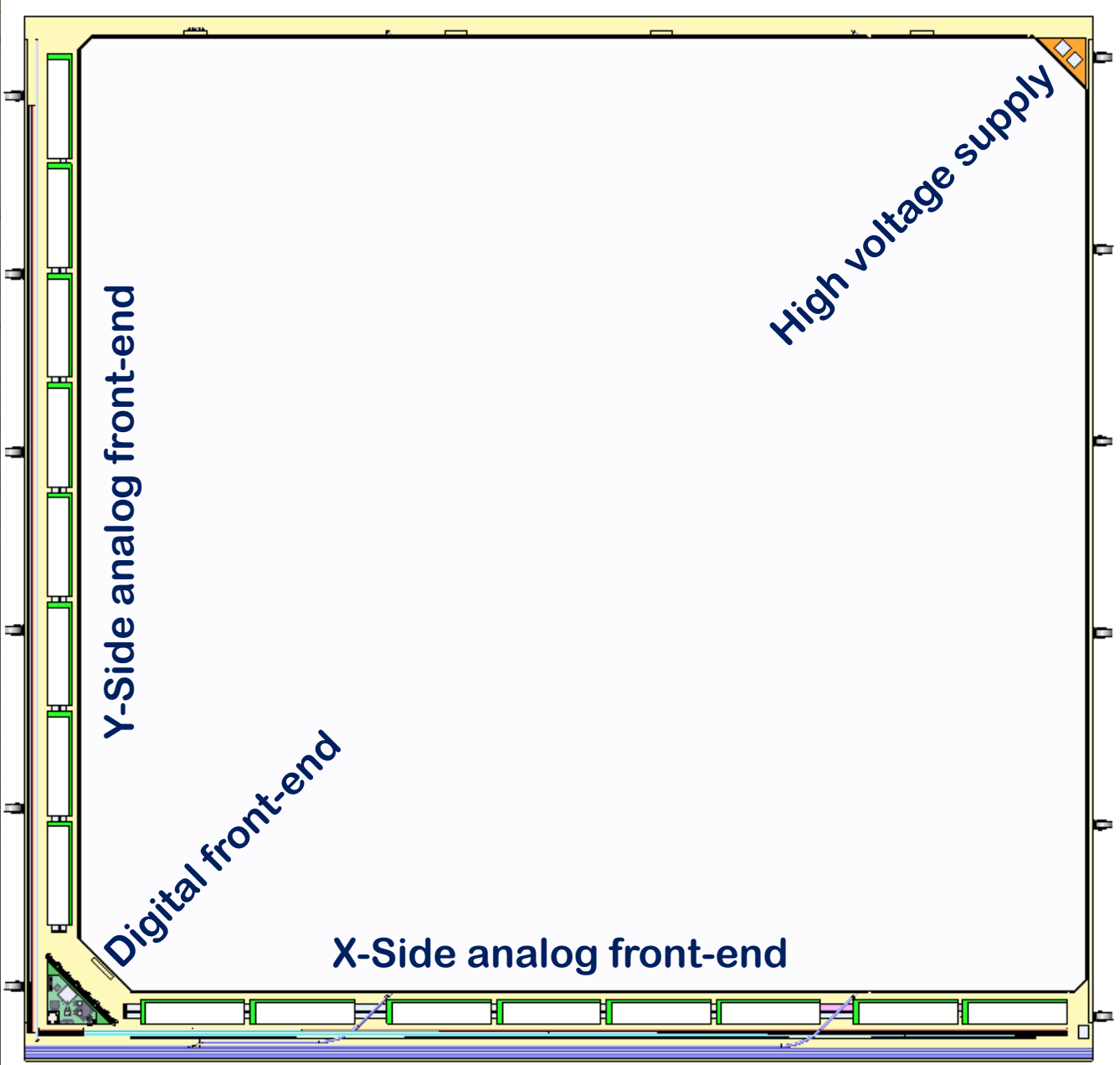


Components of ICAL electronics

- Analog Front-end based on Anusparsh ASIC
- Digital Front-end (RPCDAQ) using a TDC ASIC
- Trigger System
- Global services, calibration and synchronisation
- Network and backend hardware
- Backend software
- Power supplies
- Electronics integration



RPC and its readout components



HMC preamps for ICAL test stands

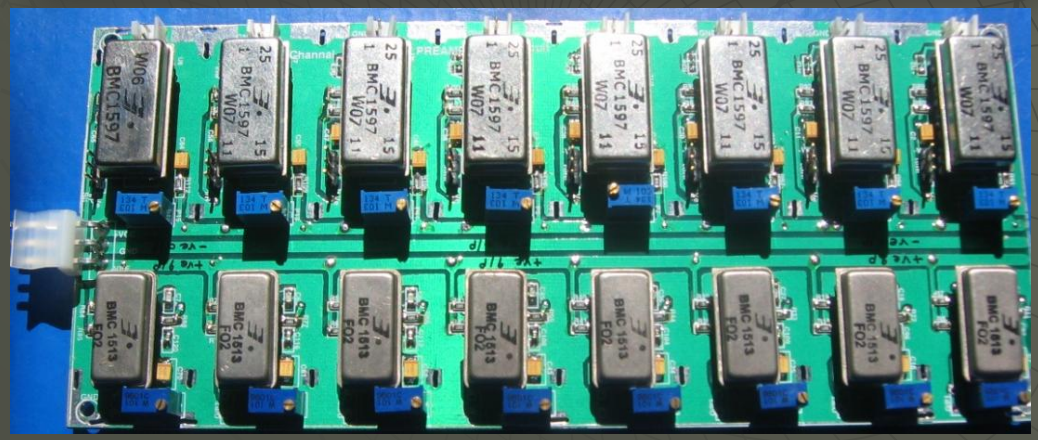
BMC1595
(Negative In – Negative Out)

BMC1596
(Positive In – Positive Out)

BMC1597
(Positive In – Dual Out)

BMC1598
(Negative In – Dual Out)

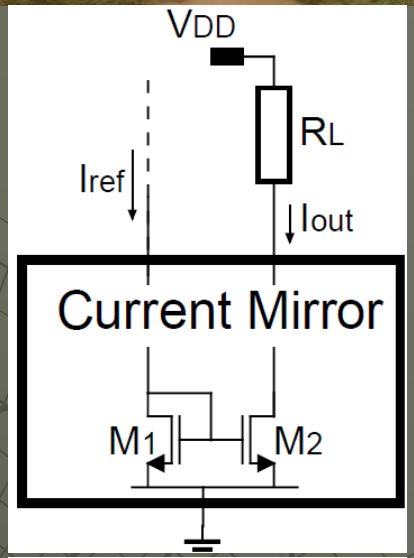
BMC1513
(Negative In – Negative Out)

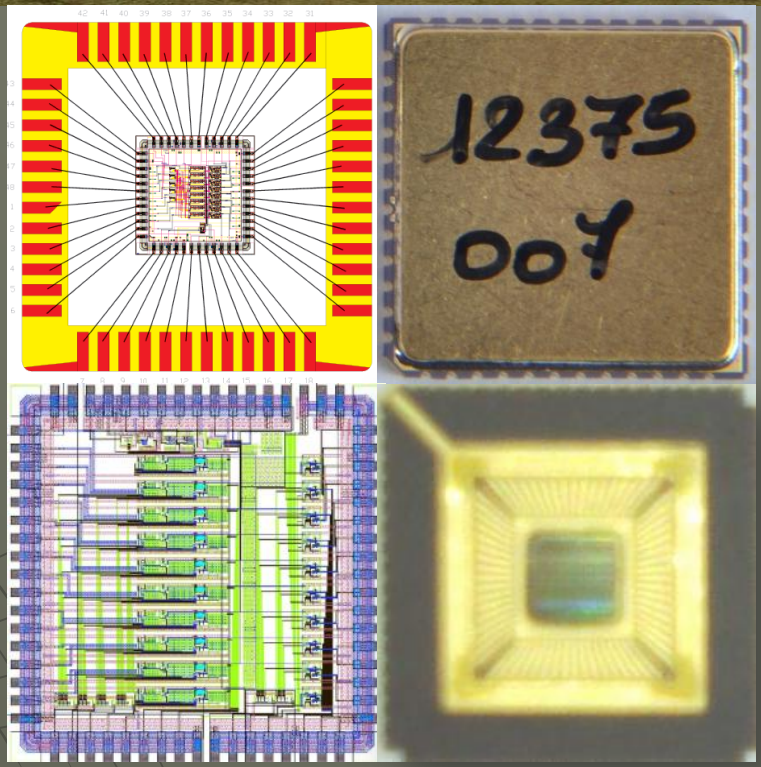


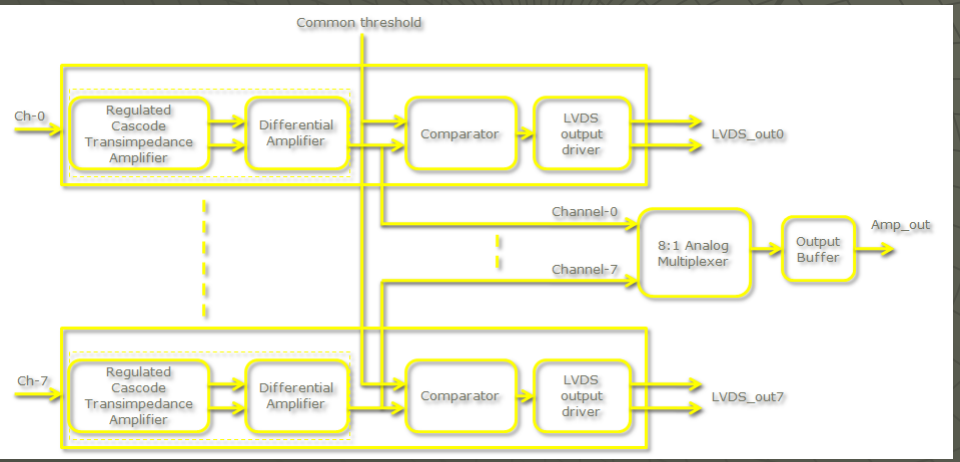
- Input & Output impedance: 50Ω
- Nominal gain: 10
- Rise time: ~1.2 ns
- Bandwidth: 350MHz
- Package: 22-pin DIP
- Power Supply : ± 6V
- Power Consumption: 110mW

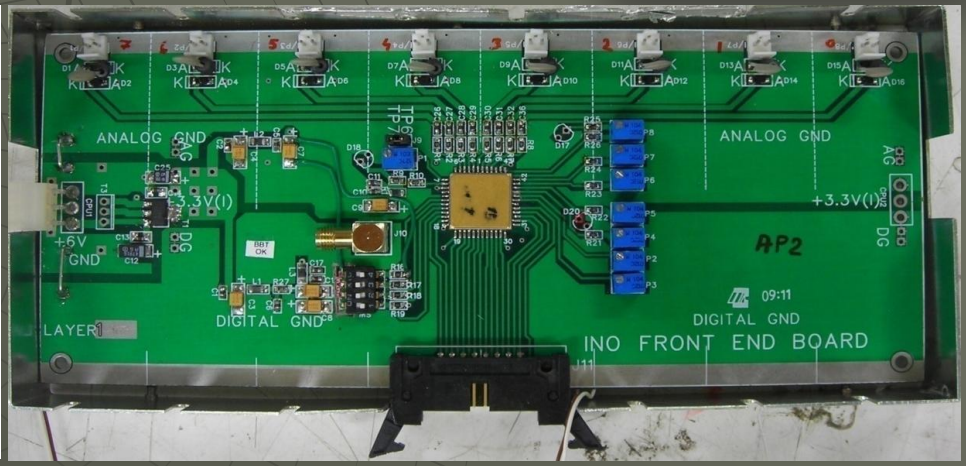
Transimpedance AFE ASICs

- Process: AMSc35b4c3 (0.35µm CMOS) by IMEC, Belgium
- Input dynamic range: 18fC(1µA)–1.36pC(80µA)
- Input impedance: 45Ω @350MHz
- Amplifier gain: 8mV/µA
- 3-dB Bandwidth: 274MHz
- Rise time: 1.2ns
- Comparator's sensitivity: 2mV
- LVDS drive: 4mA
- Power per channel: ~20mW
- Package: CLCC(48/68-pin)
- Chip area: 13mm²



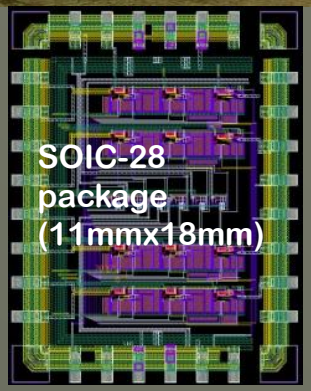


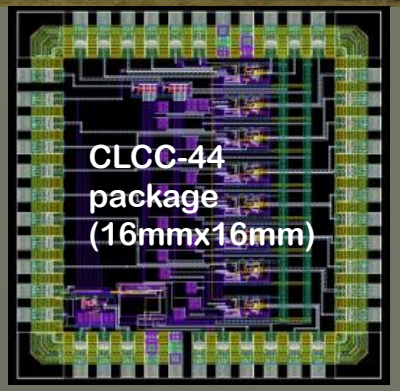


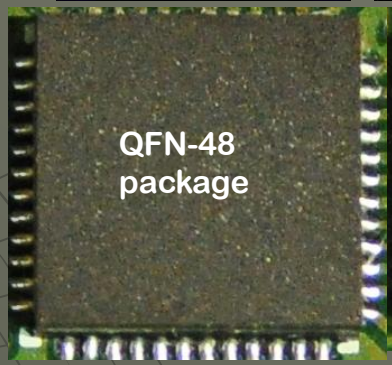


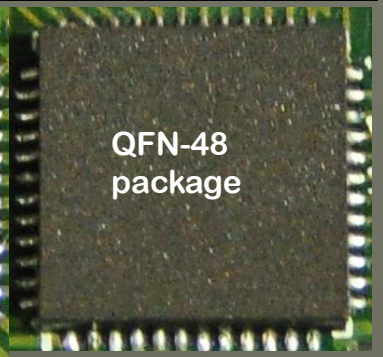
Voltage amplifier ASICs

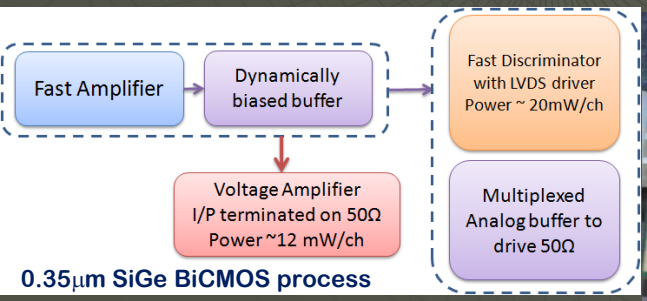
- An 8-channel AFE board using two, 4-channel preamplifier and one, 8-channel discriminator ASICs designed, fabricated and extensively tested on RPC test stands at BARC and TIFR.
- Horizontal mounting in the RPC tray agreed upon for the Engineering Module as the board dimension couldn't reduced below 200mm × 45mm.
- Small volume order for the ASIC chipset in QFN package and boards produced.
- Chip packing options, board manufacturer development, automatic assembly lines and test equipment are being planned.

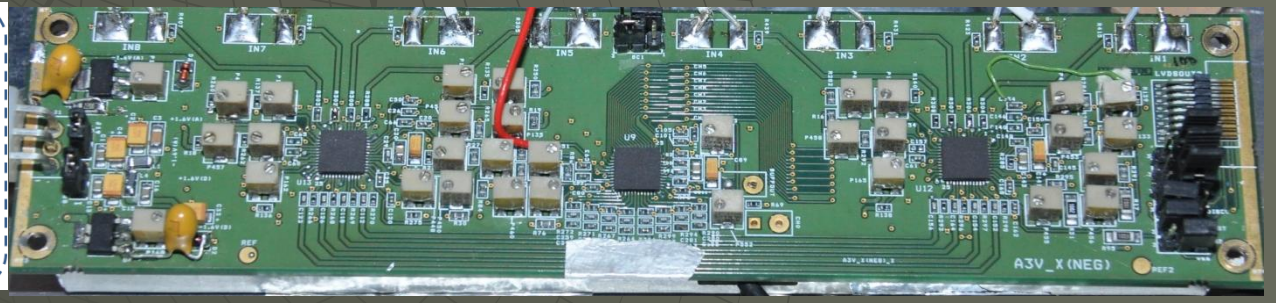




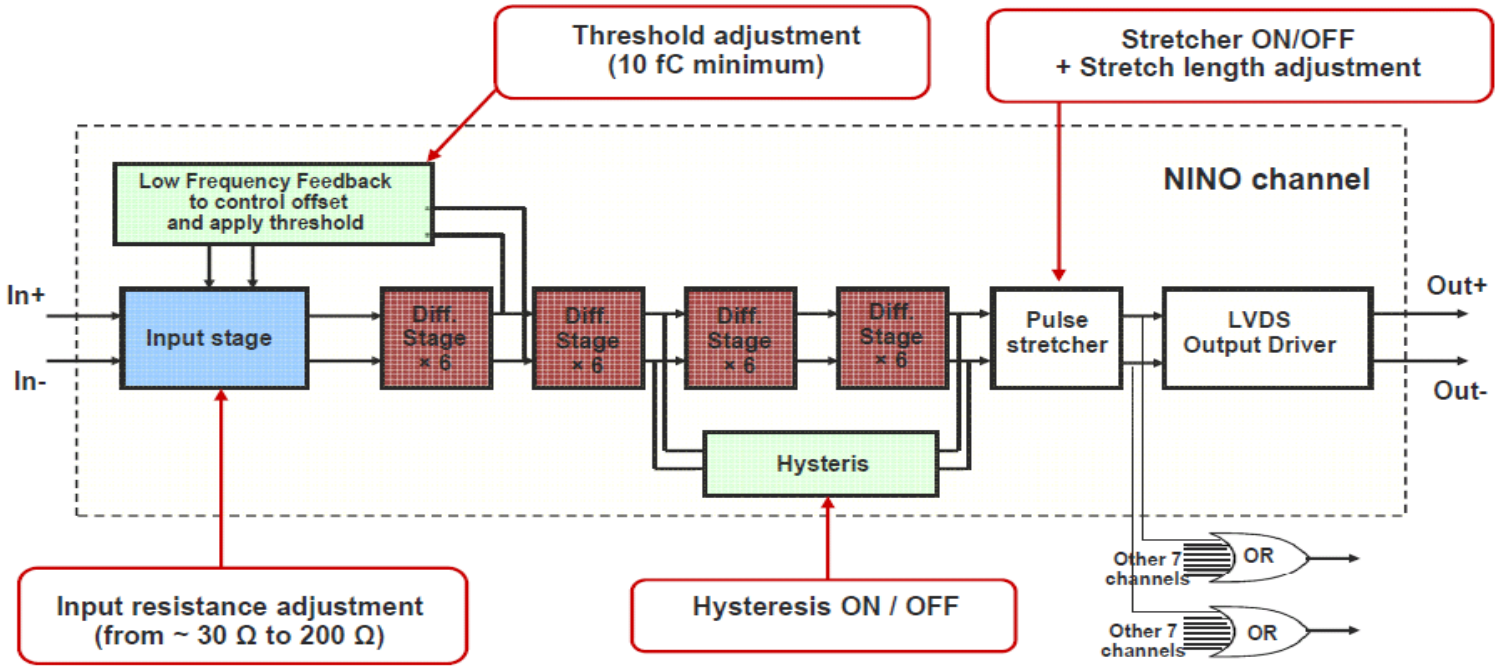


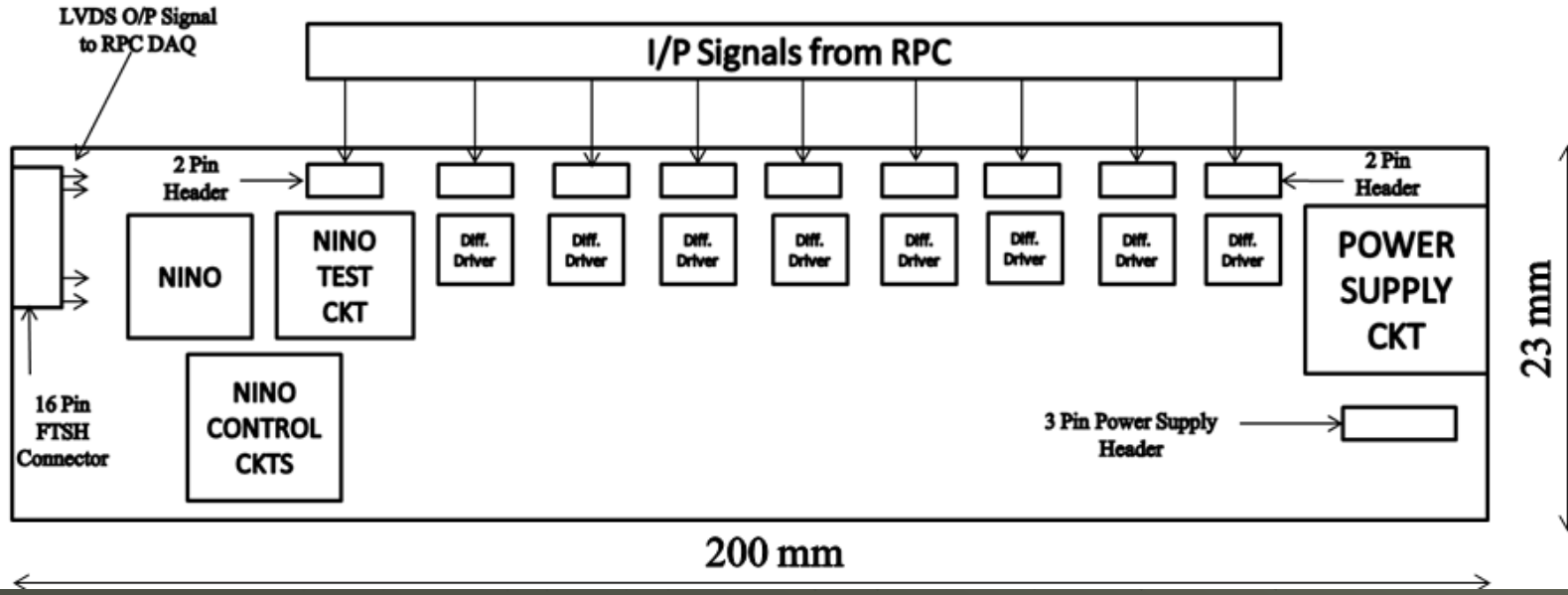






NINO based AFE board



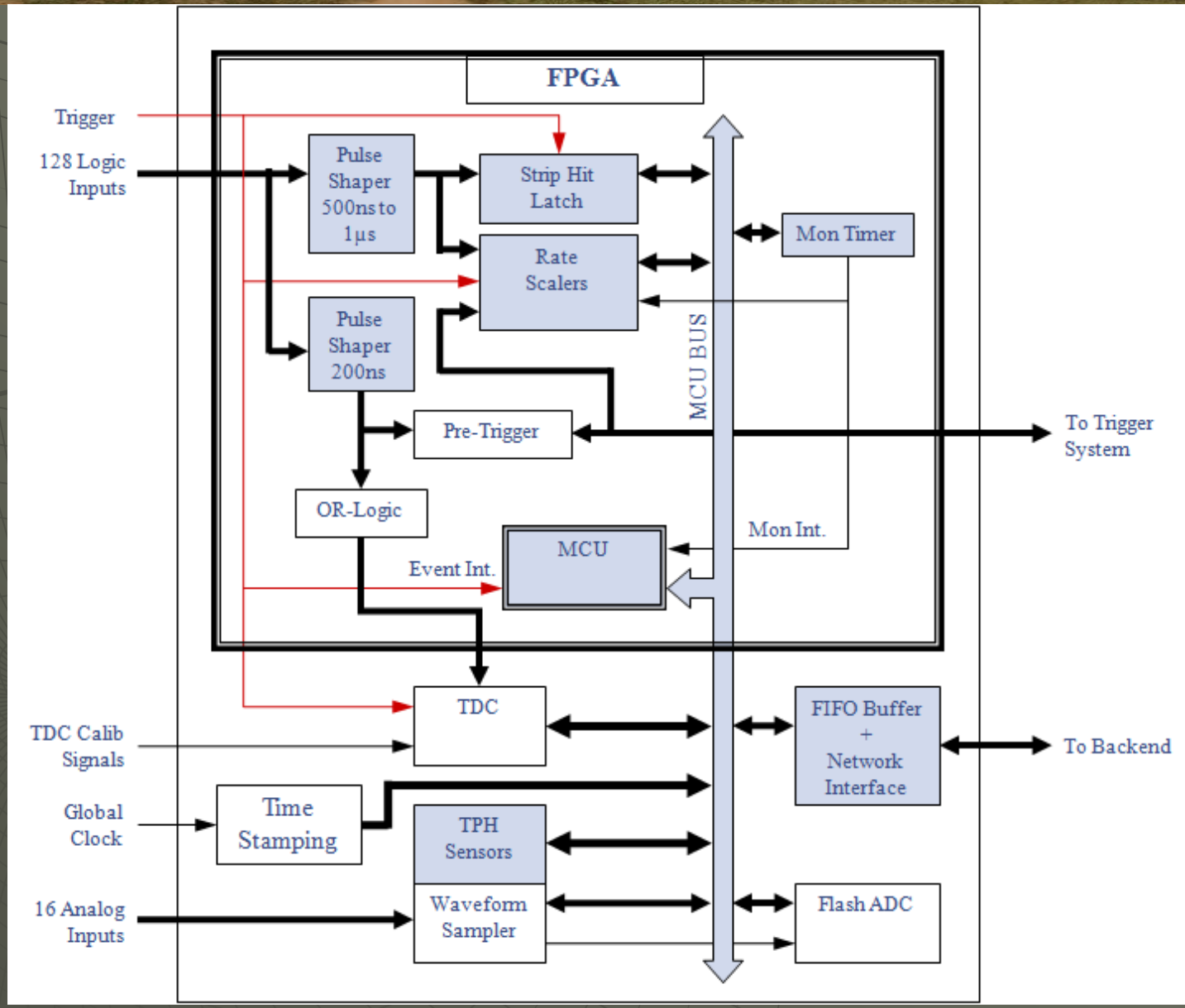


Performance comparison

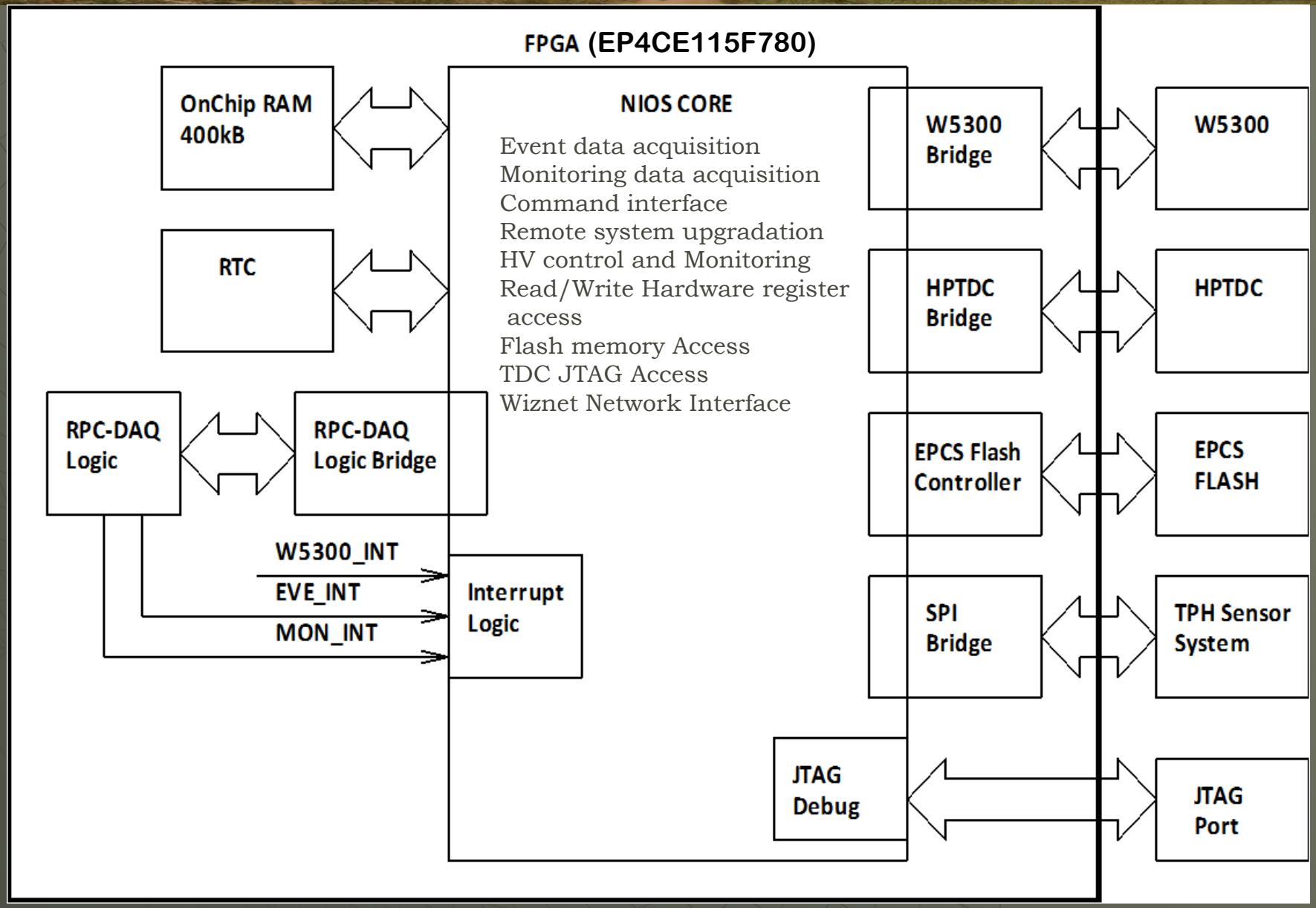
Preamplifier Solutions	Total Events	Threshold	Efficiency (%)	Noise Rate (Hz)
HMC	1073	-20mV	92	55
Anusparsh v3	10673	25mV	90	33
NINO ALICE Board (Diff Driver Gain 1)	5997	10fC	91	43
NINO ALICE Board (Diff Driver Gain 1.5)	666	10fC	91	189
NINO 8 channel Preamp Board (Diff Driver Gain 1)	1634	80fC	92	45

DFE module – the workhorse

- Unshaped, digitized, LVDS RPC signals from 128 strips (64x + 64y)
- 16 analog RPC signals, each signal is a summed or multiplexed output of 8 RPC amplified signals.
- Global trigger
- TDC calibration signals
- TCP/IP connection to backend for command and data transfer



Soft-core processor



ICAL TDC specifications

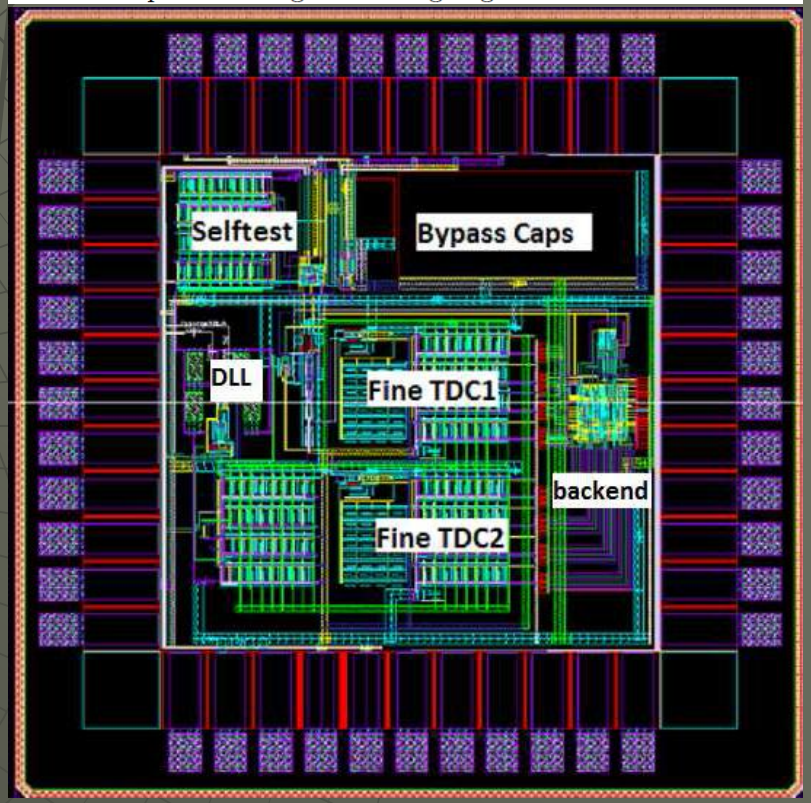
Parameter	Specification
Number of channels	8 or 16
Least count	200ps
Dynamic range	2μs (essential), 32μs (desirable)
Number of bits	14 (essential), 18 (desirable)
Type	Common stop
Hits	Single hit (essential), multi hit (desirable)
Double hit resolution	5-10ns
Readout buffer size	128 words (maximum)
Signal and control inputs	LVDS and LVTTL respectively
DNL/INL	100ps (typical)
Power rail	3.0 to 3.6V (suggested)
Control and readout interface	SPI (essential), SPI + parallel (desirable)

ASIC based TDC device

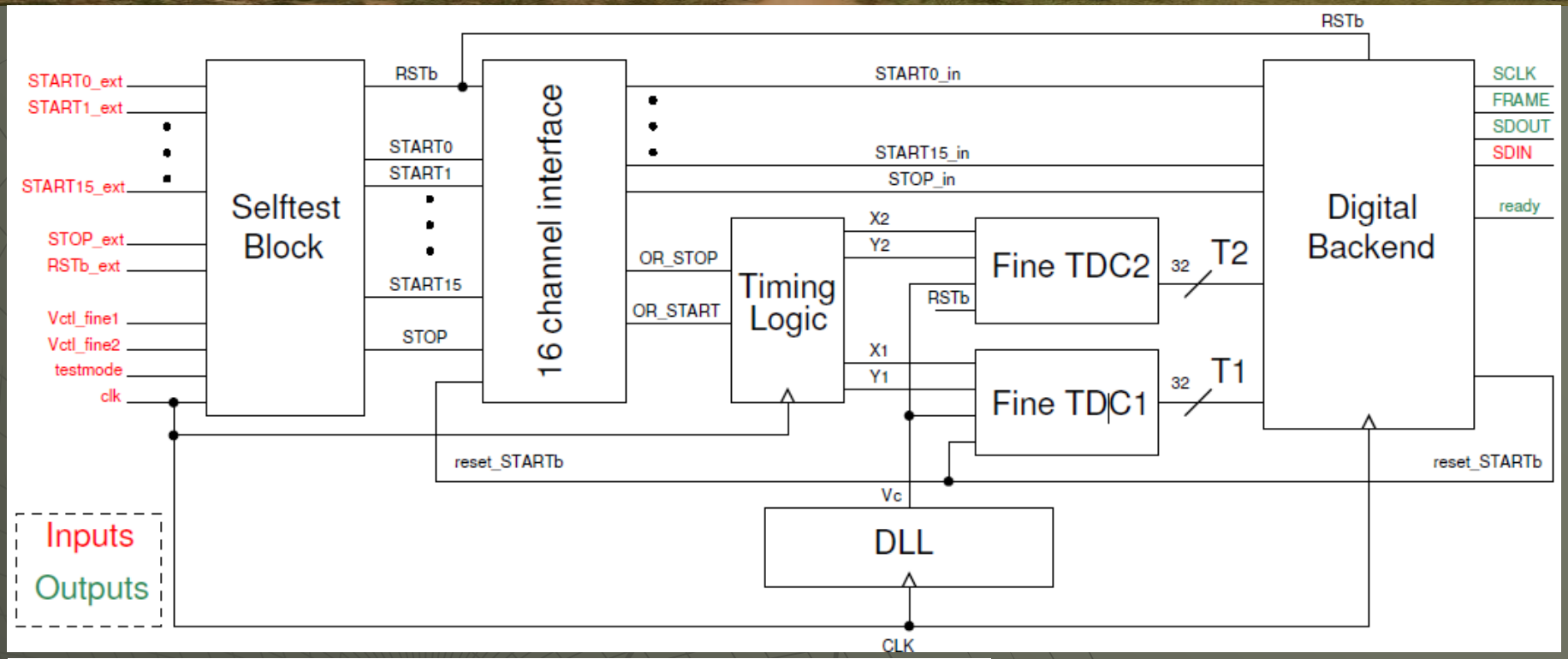
- **Principle**
  - Two fine TDCs to measure start/stop distance to clock edge (T_1, T_2)
  - Coarse TDC to count the number of clocks between start and stop (T_3)
  - TDC output = $T_3+T_1-T_2$
- **Specifications**
  - 19 bit parallel output
  - Clock period, T_c = 4ns
  - Fine TDC interval, $T_c/32$ = 125ps
  - Coarse TDC output: 14 bits
  - Fine TDC output: 5 bits
  - Coarse TDC interval: $2^{14} * T_c$ = 65.536ms

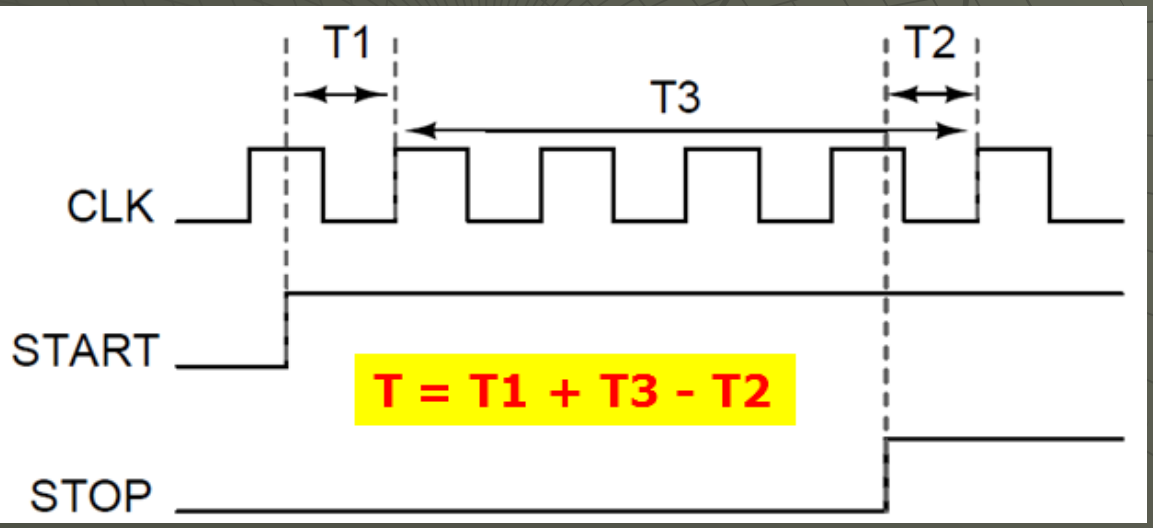
Resolution	:	125 ps
Range	:	65.536 μs
Reference Frequency	:	10 MHz
Voltage Supply	:	1.2V
Technology	:	UMC130 (130 nm process)
No: of Channels	:	16 STARTs (hits), 1 STOP (trigger)
Chip read out	:	SPI

Zero deadtime between hits across different channels.
Time stamp both rising and falling edges.



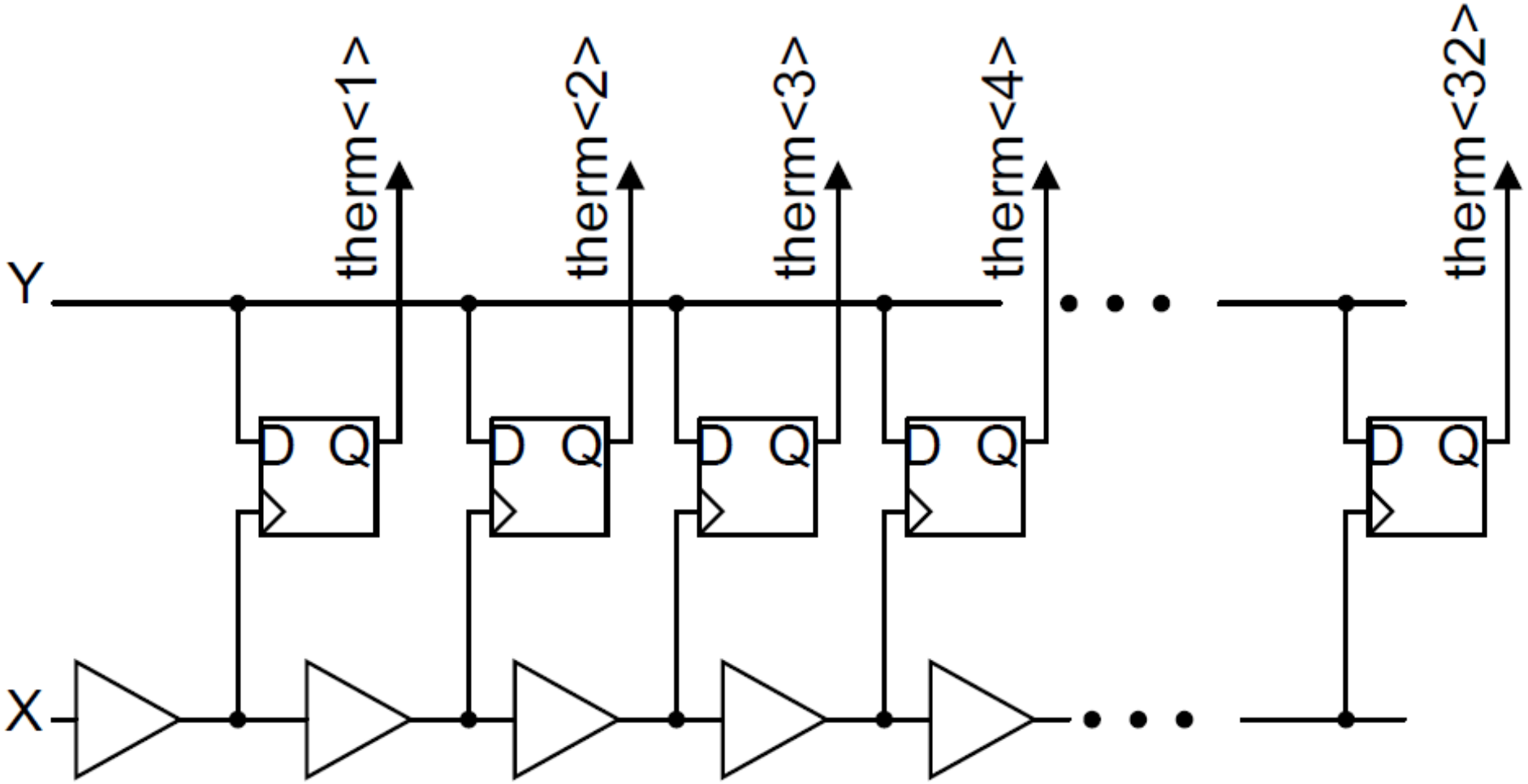
Overall block diagram





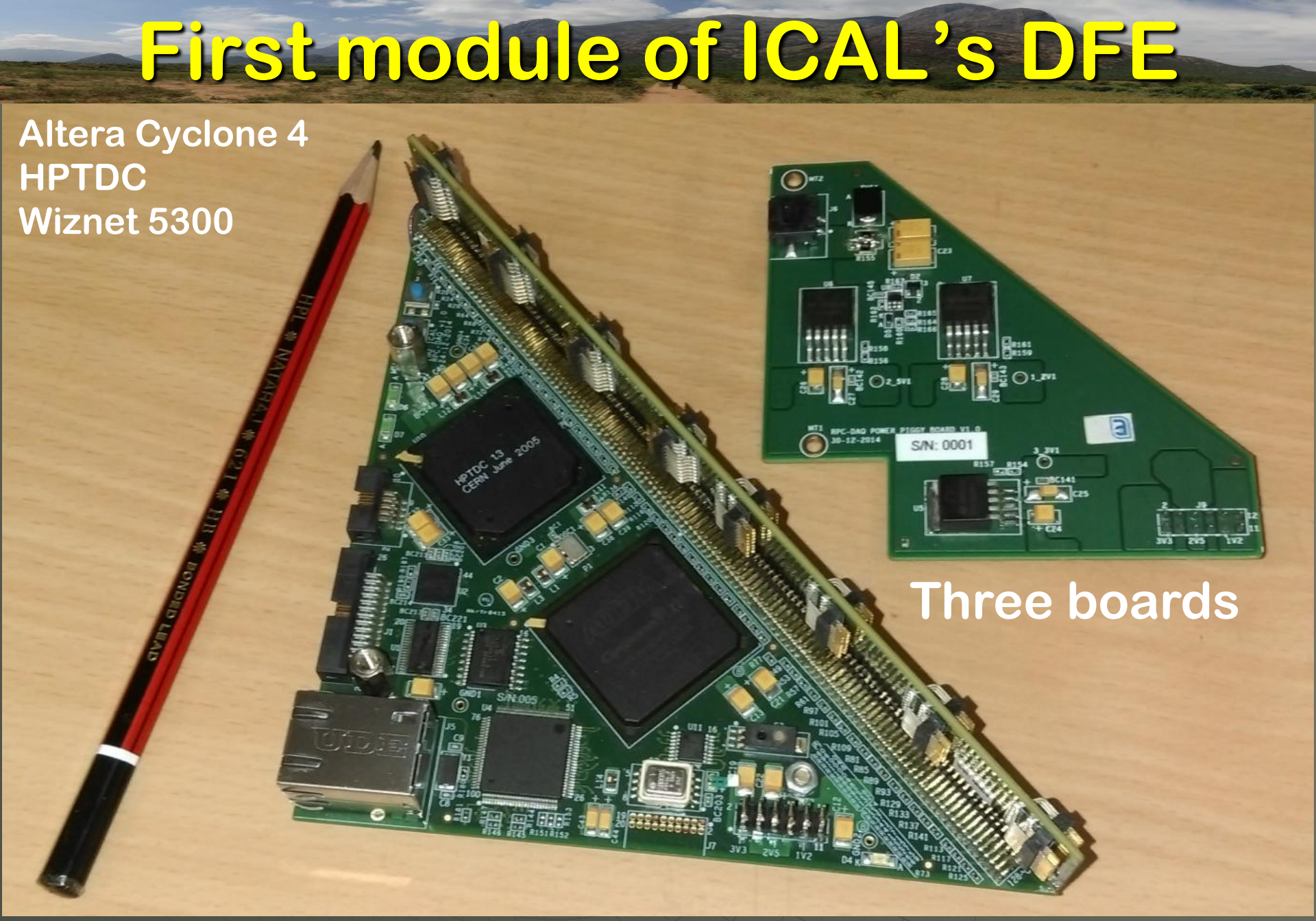
Principle of timing measurement

Implementation of fine TDC

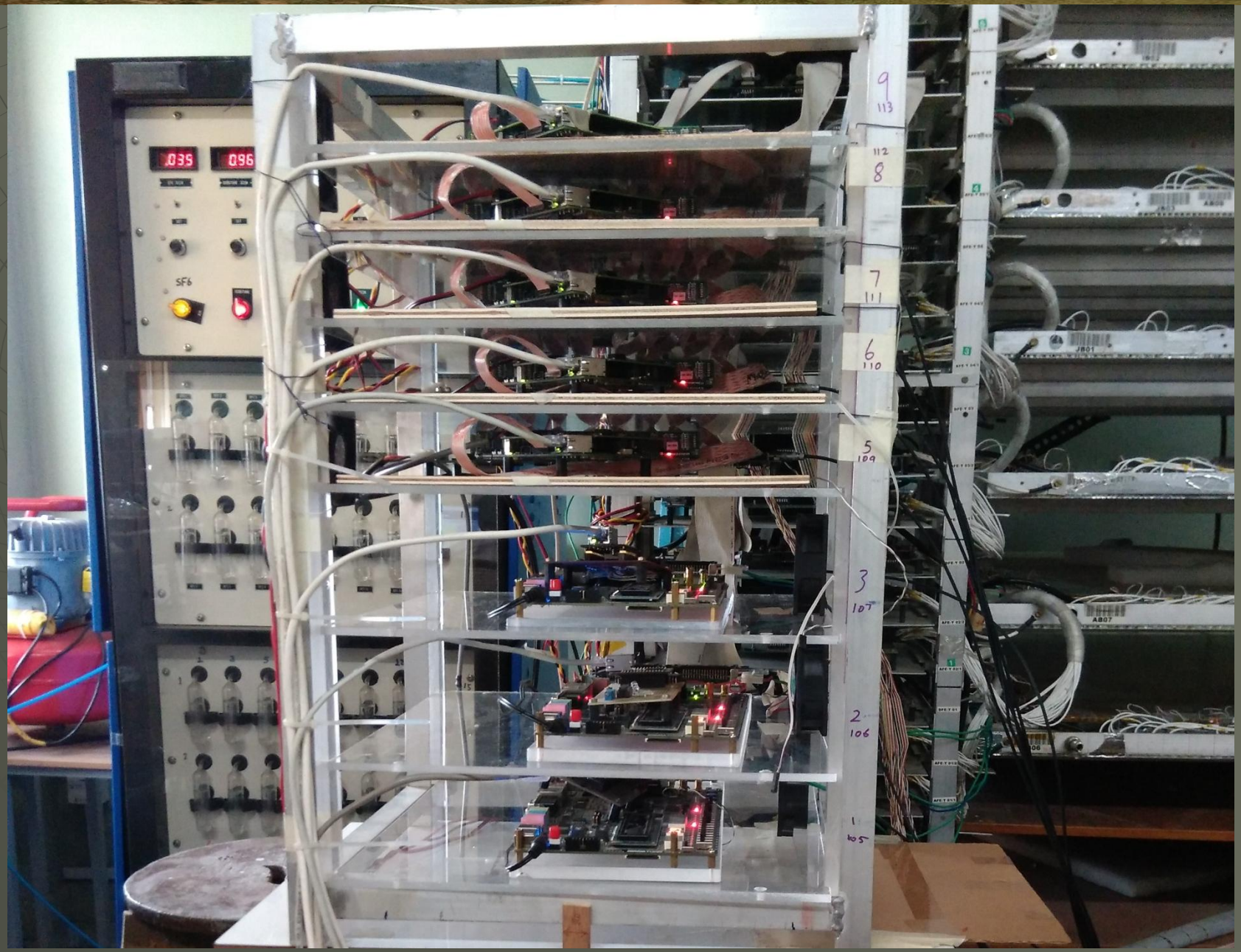


$$(j-1)T_d \leq T_{xy} \leq jT_d$$

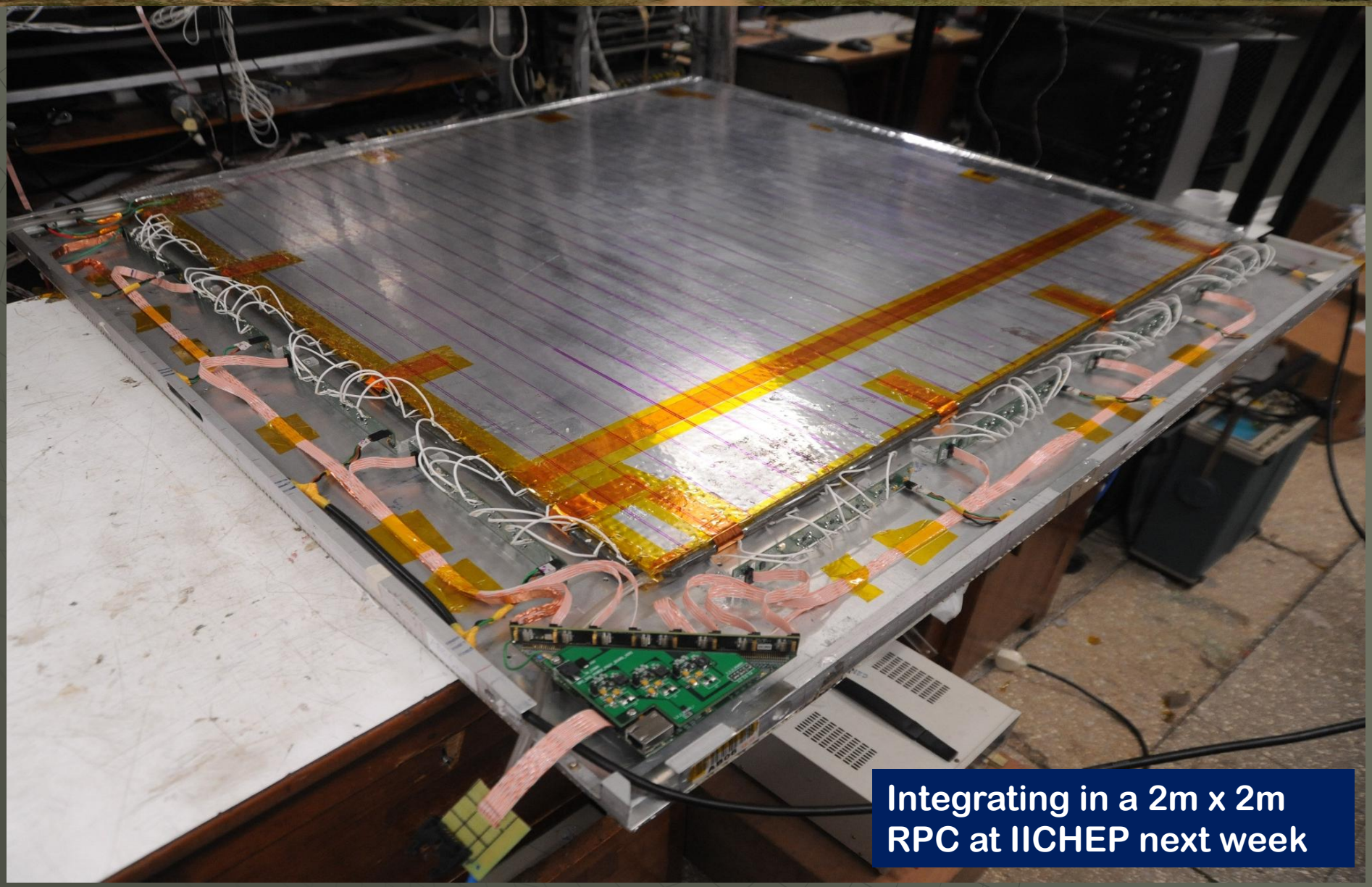
First module of ICAL's DFE



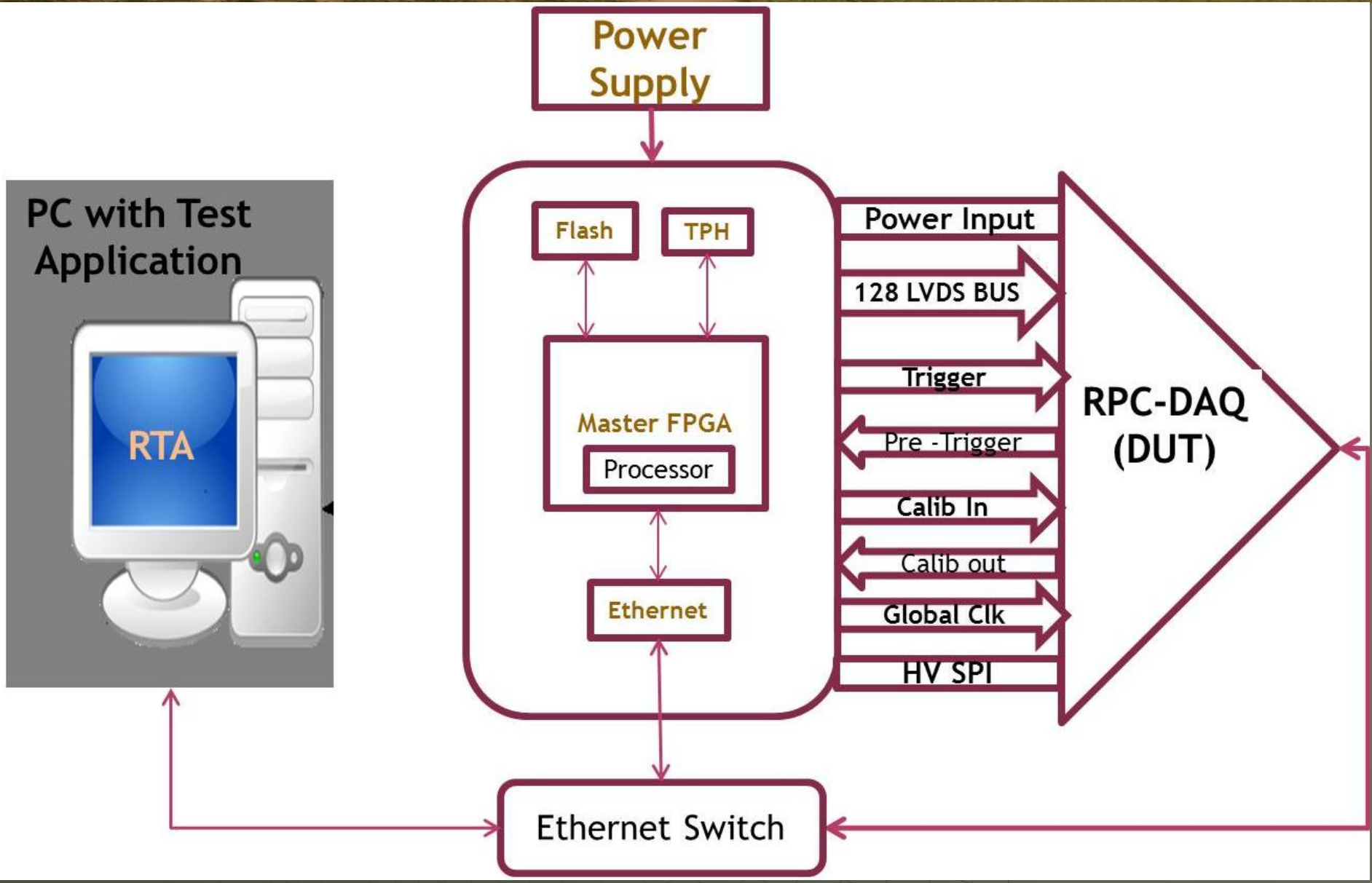
ICAL DFEs in the RPC test stand



An RPC with NINO AFEs and a DFE

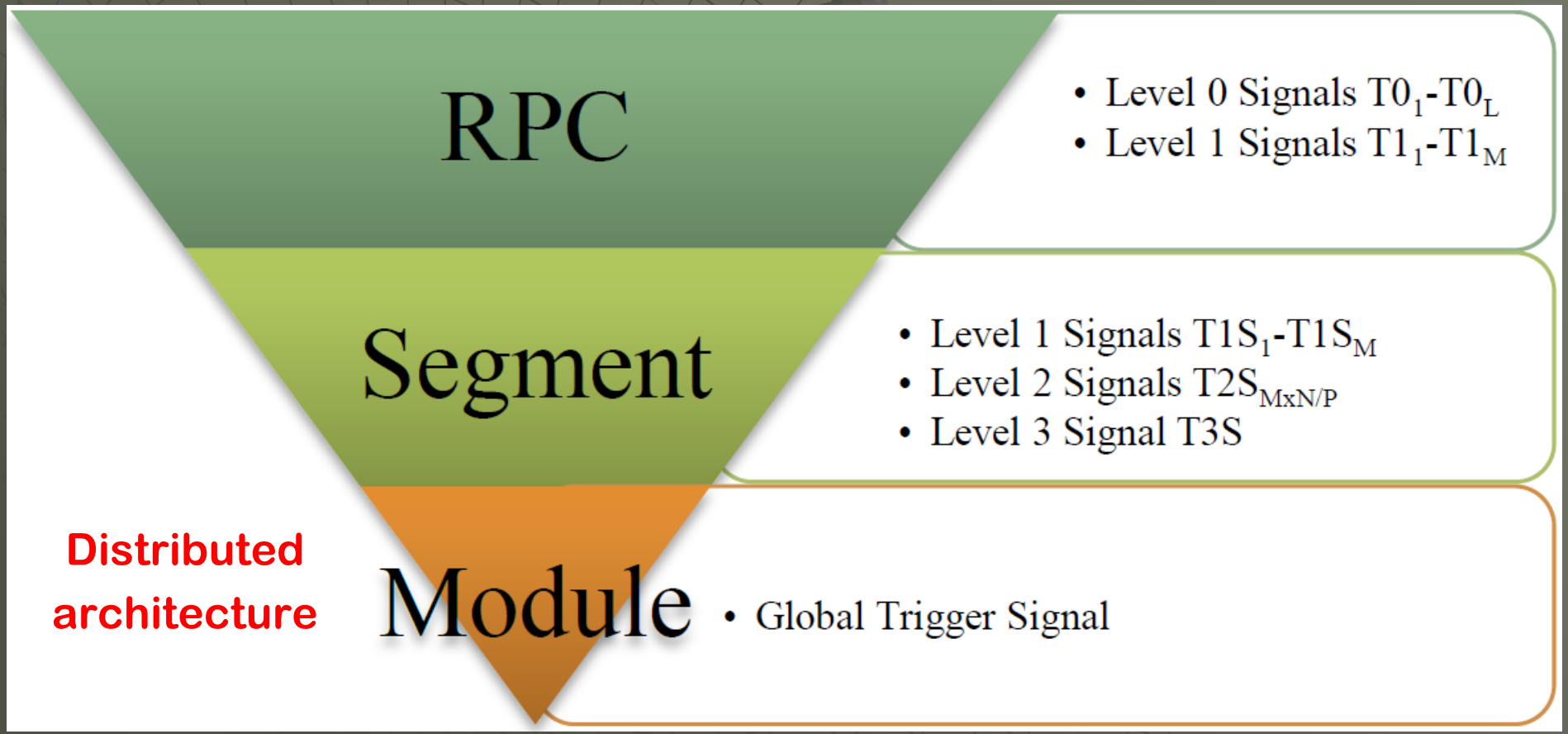


DFE test jig


Power Supply
PC with Test Application
RTA
Flash
TPH
Master FPGA
Processor
Ethernet
Power Input
128 LVDS BUS
Trigger
Pre -Trigger
Calib In
Calib out
Global Clk
HV SPI
RPC-DAQ (DUT)
Ethernet Switch

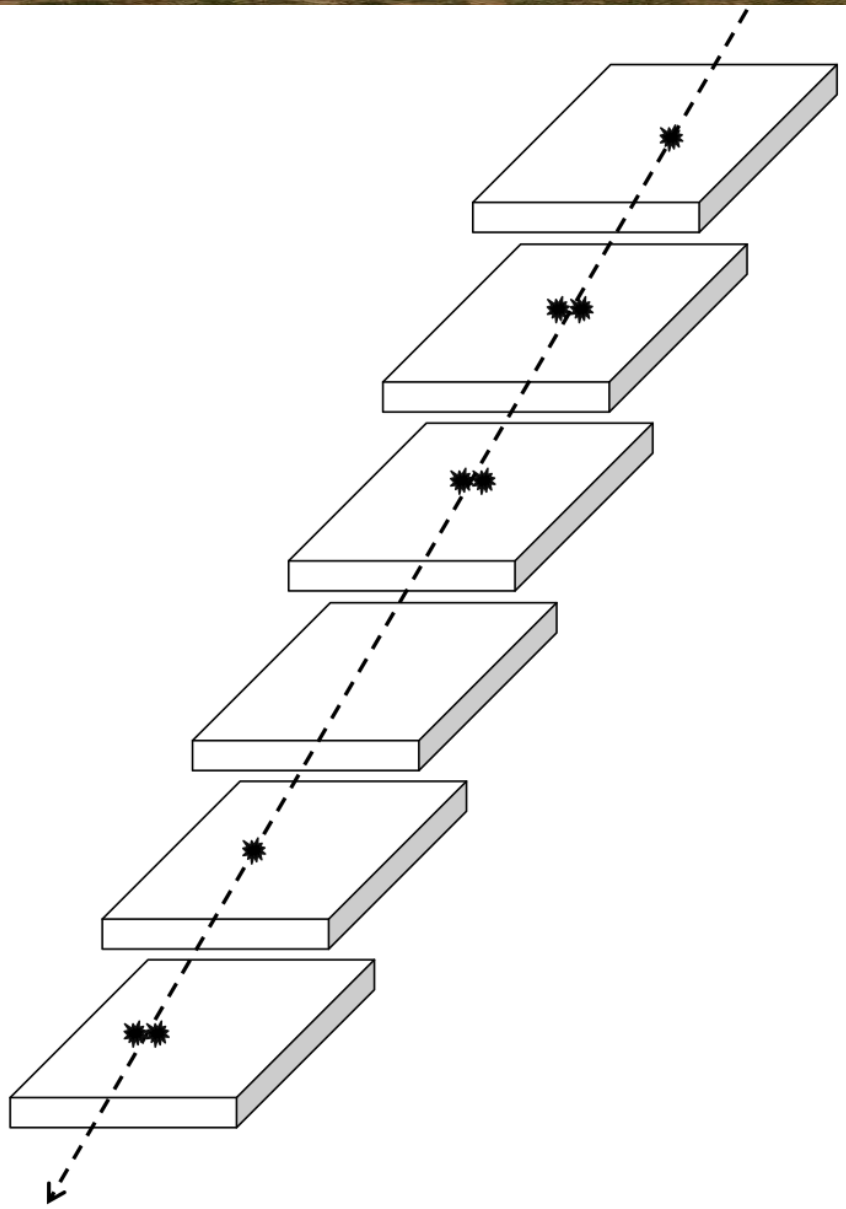
ICAL trigger scheme

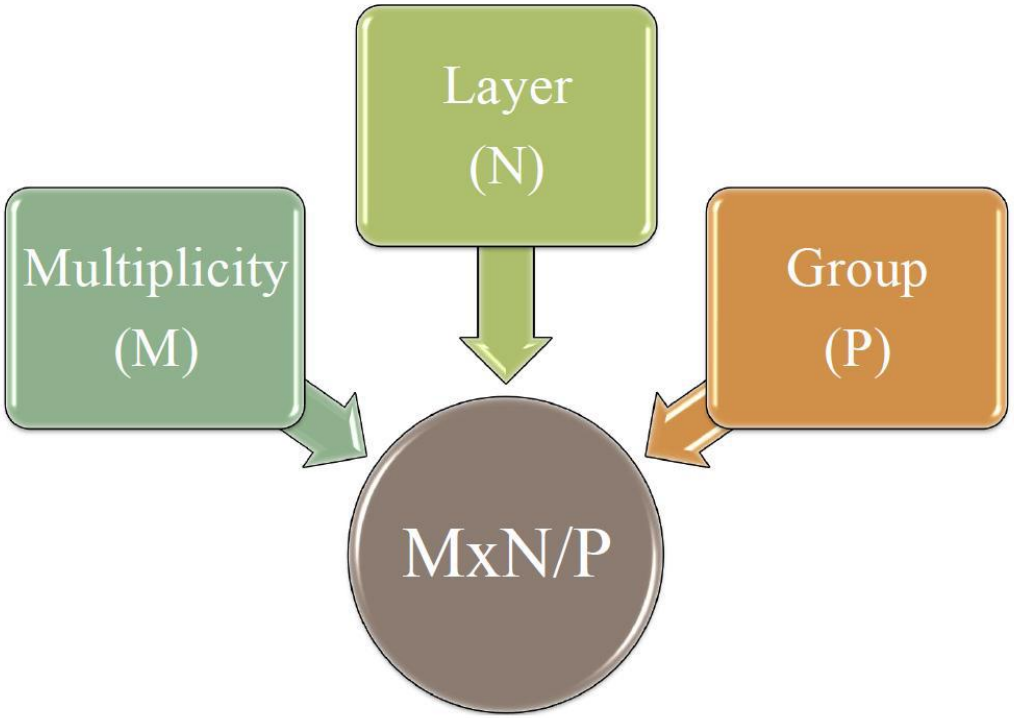
- *Insitu* trigger generation. Autonomous; shares data bus with readout system
- For ICAL, trigger system is based only on topology of the event; no other measurement data is used
- Huge bank of combinatorial circuits; Programmability is the game, FPGAs, ASICs are the players



Distributed architecture

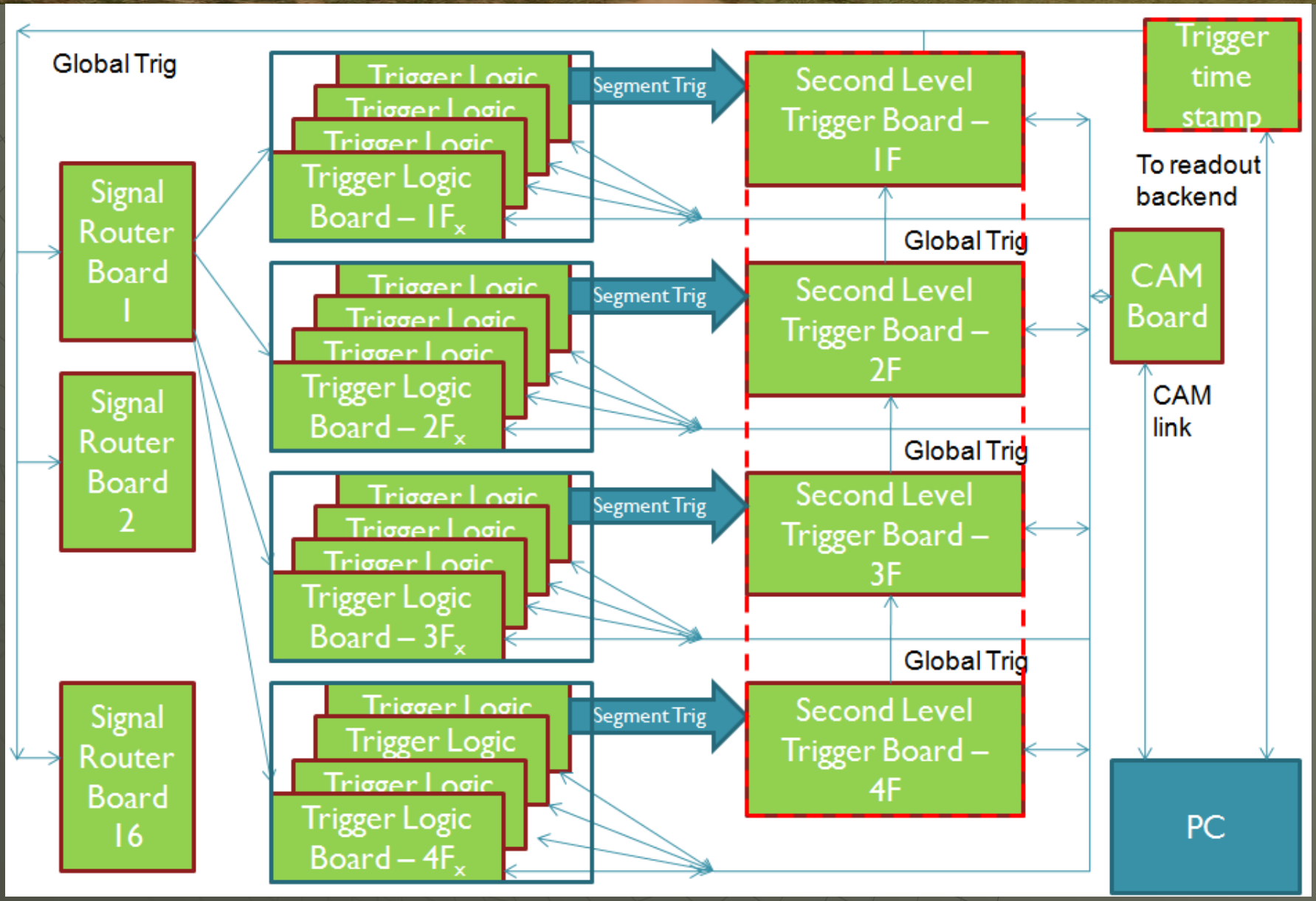
Trigger criteria



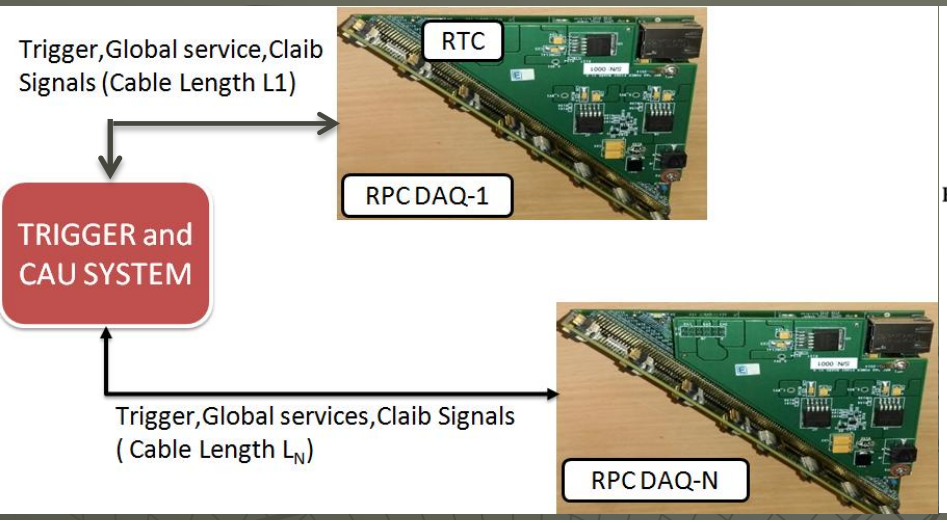


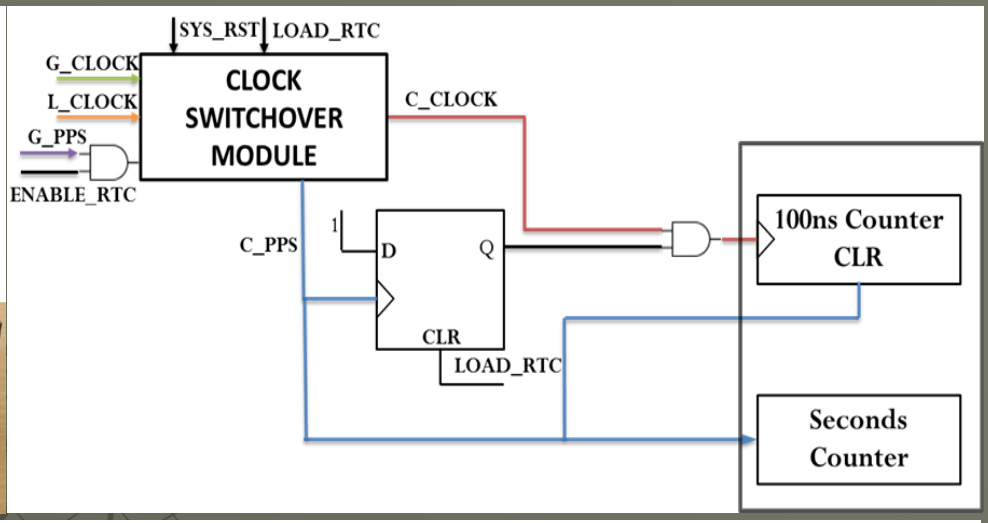
	Non-overlapped			Overlapped
RPC Strip Rate	Chance Rate for Full Trigger	Chance Rate for Partial Trigger	Total Chance Coincidence Rate	Total Chance Coincidence Rate
250 Hz	71 Hz	841 Hz	912 Hz	319 Hz
50 Hz	0.023 Hz	0.269 Hz	0.292 Hz	0.102 Hz

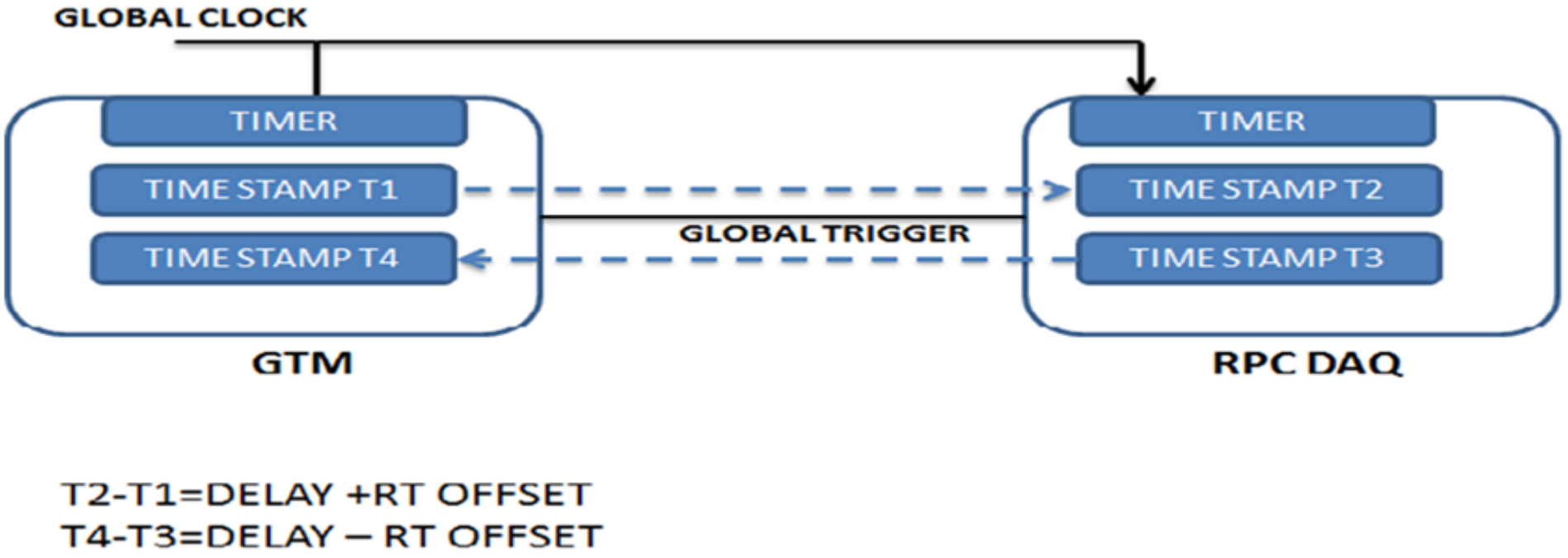
Trigger system for ICAL-EM



Calibration and synchronisation



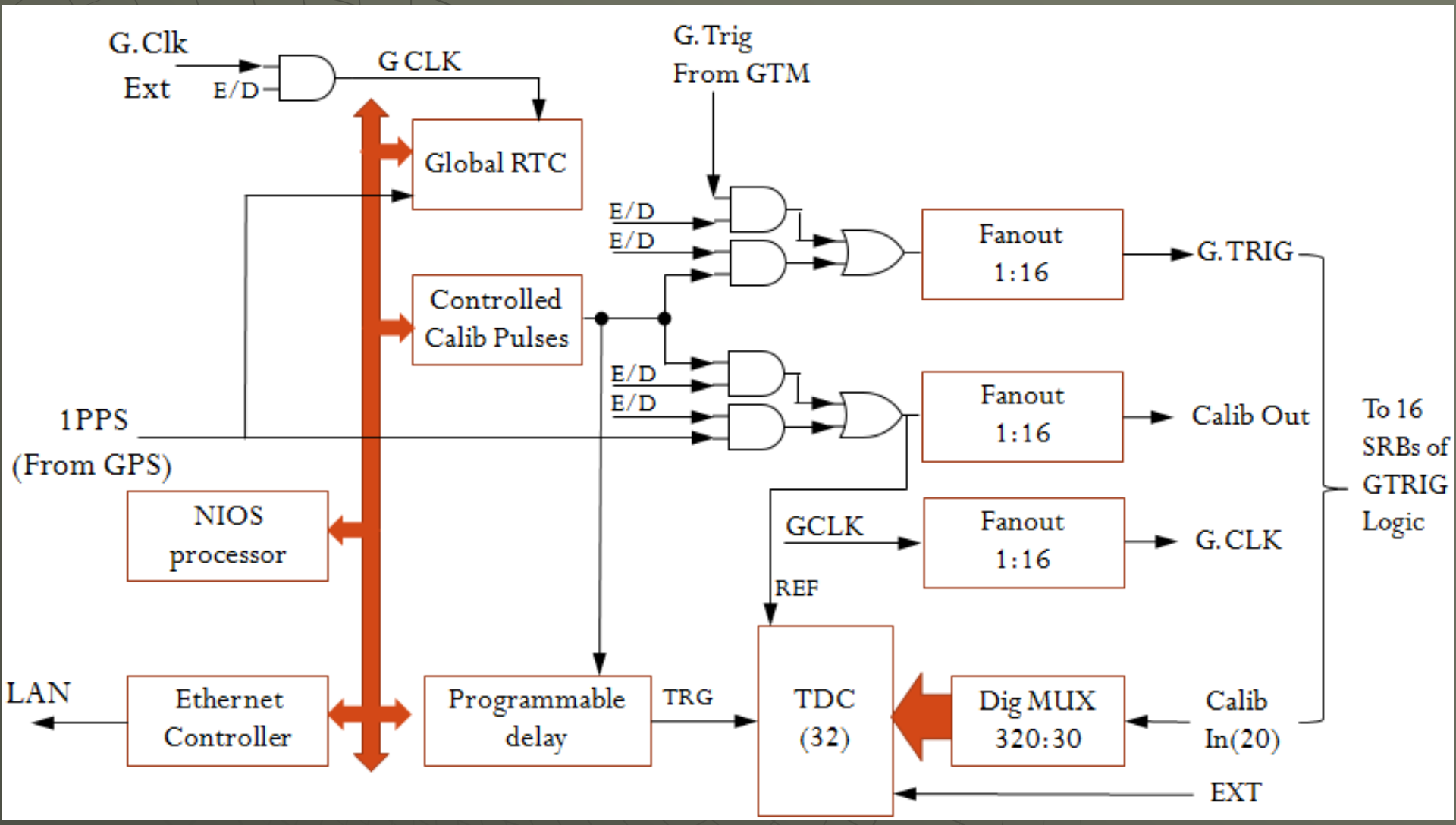




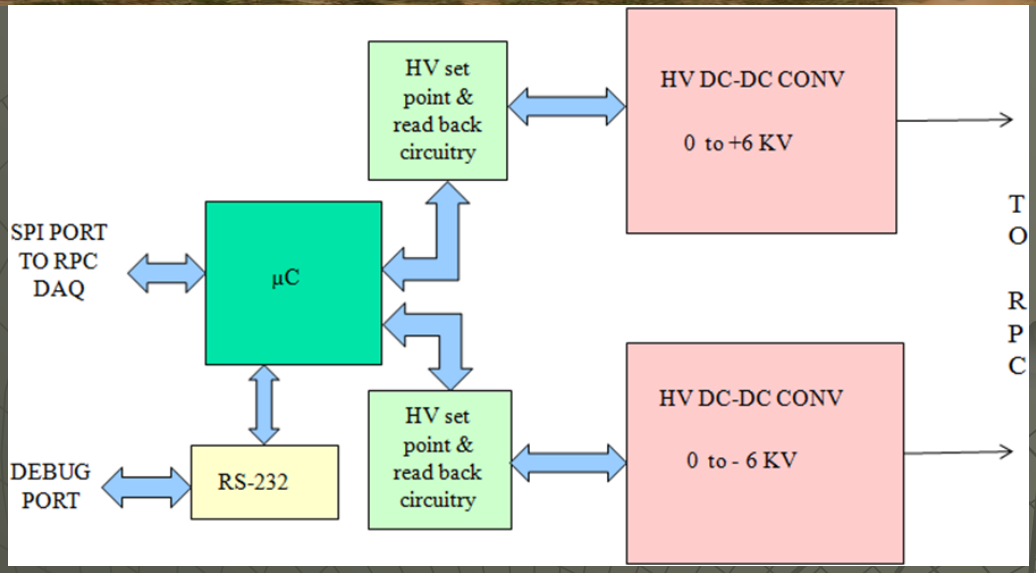
T2-T1=DELAY +RT OFFSET

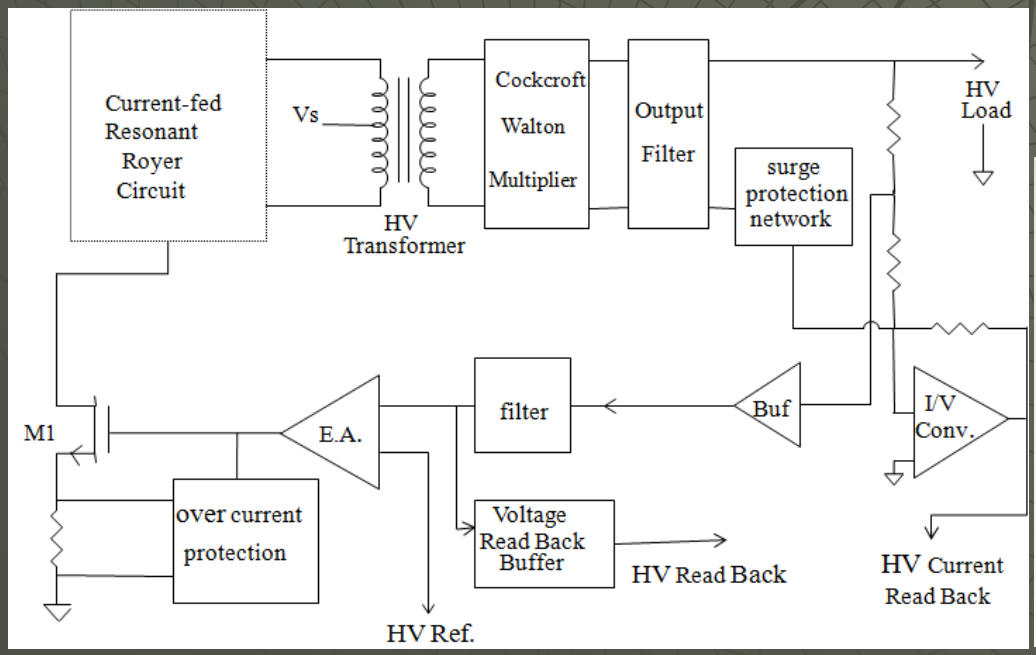
T4-T3=DELAY – RT OFFSET

Functional blocks of calibration unit

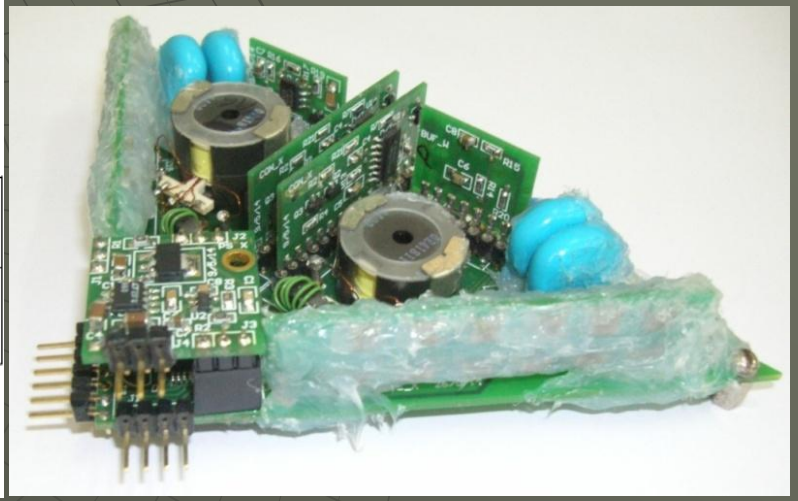


High voltage power supply

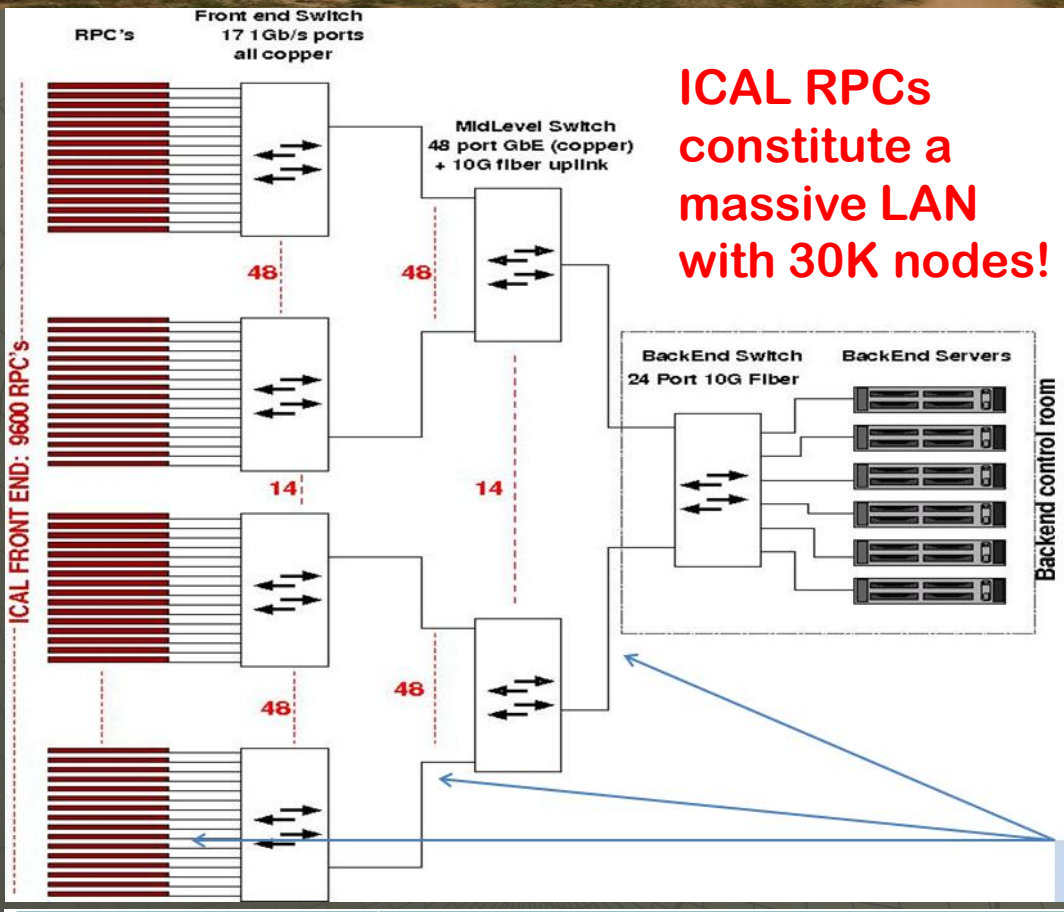




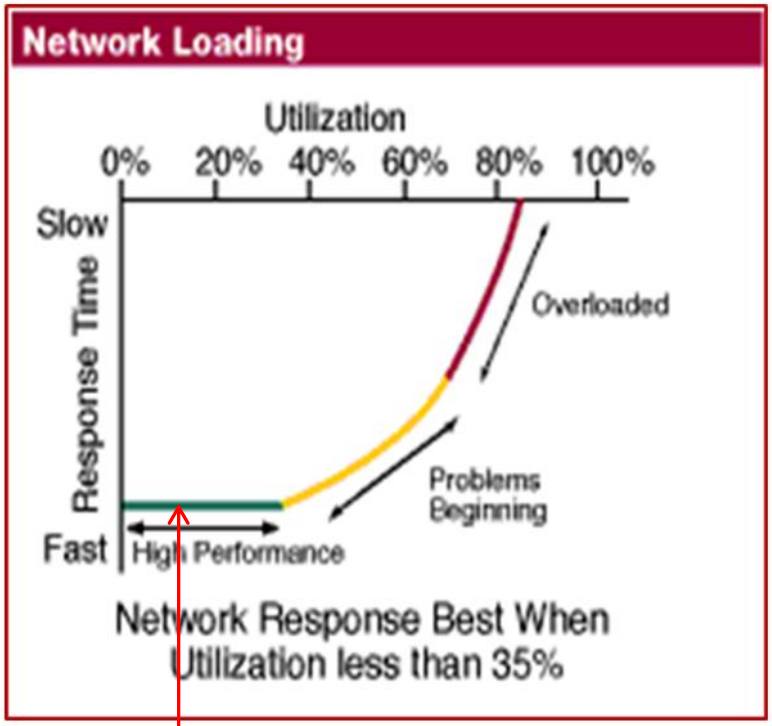
- Output voltage adjustable in the range ± 0-6KV (to generate 0-12KV) with output current up to 2µA.
- HV load regulation: better than 0.1% F.S
- Output ripple/noise voltage: within 200 mV (p-p).
- Adjustable HV Ramp rate 10-1000 Volts/ sec, HV on/off control, HV output read back facility.
- HV load current read back facility with a resolution of 5 nA.
- Required LV Input supply: 12V @200mA
- Ambient fringe magnetic field: 500 gauss



Overview of ICAL data LAN



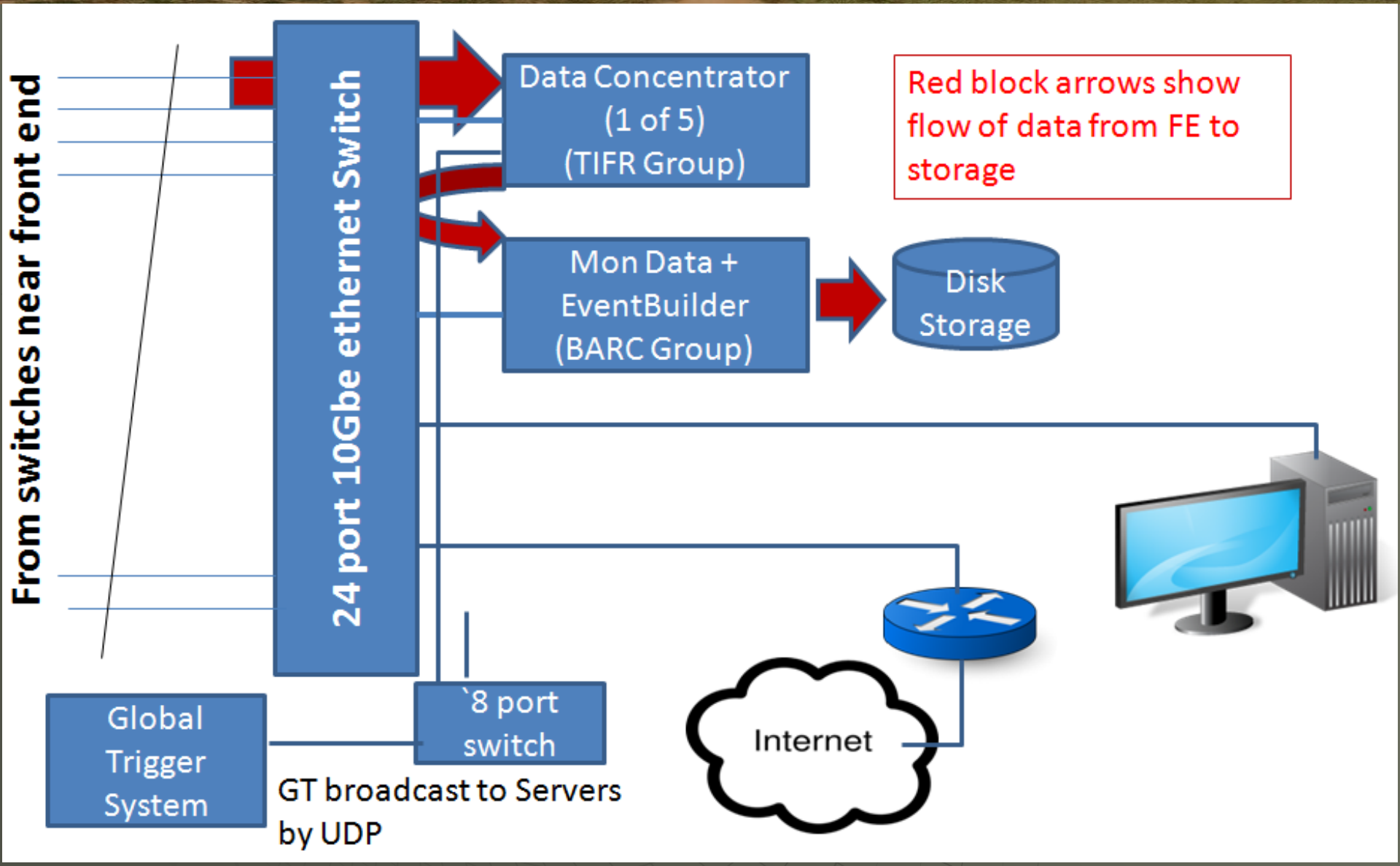
ICAL RPCs constitute a massive LAN with 30K nodes!



All cumulative traffic in high performance region

	Basic Data Size per RPC (Frond end)		Data Rate at backend	
	Without pulse profile	With pulse profile	Without Pulse Profile	With Pulse Profile
Event data (ICAL)	4384 bits	29984 bits	42.8Kbps (assuming 10Hz event rate)	292.8Kbps
Event data (ICAL-EM)	4384 bits	----------	1600Mbps (assuming 10KHz event rate)	----------
Monitor data (10s)	688 bits	3200688 bits	69 bps	312.6Kbps

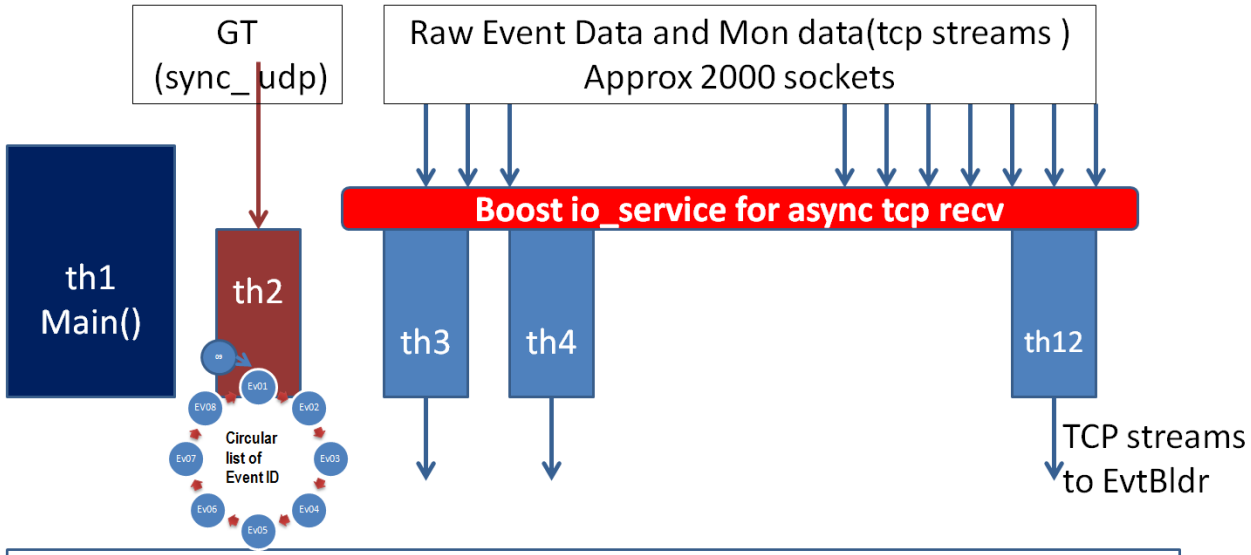
Backend hardware



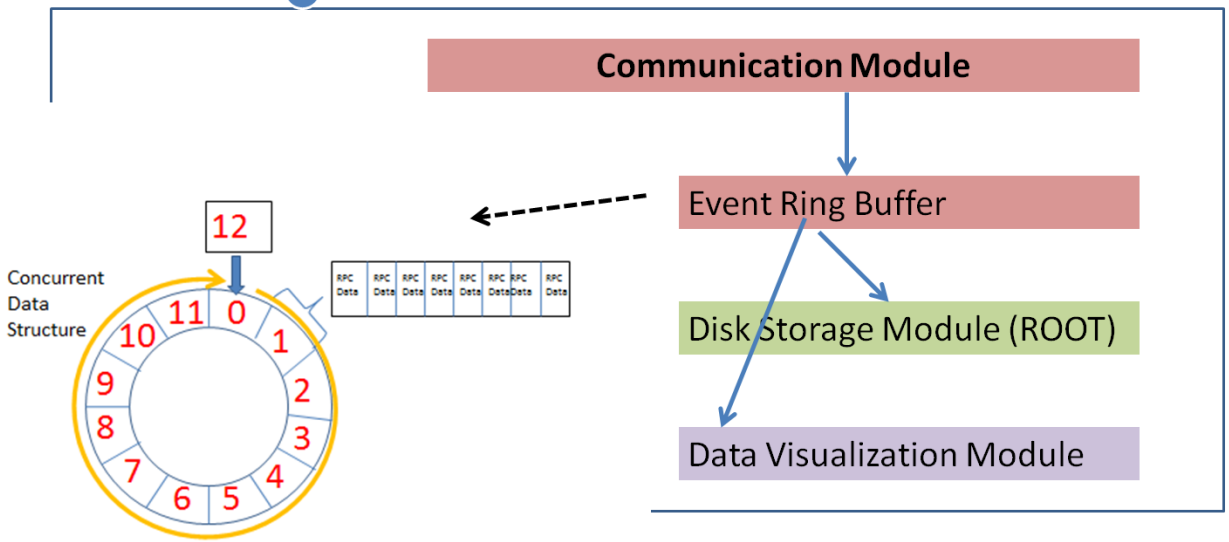
Backend data handling

Data Concentrator (TIFR Group)

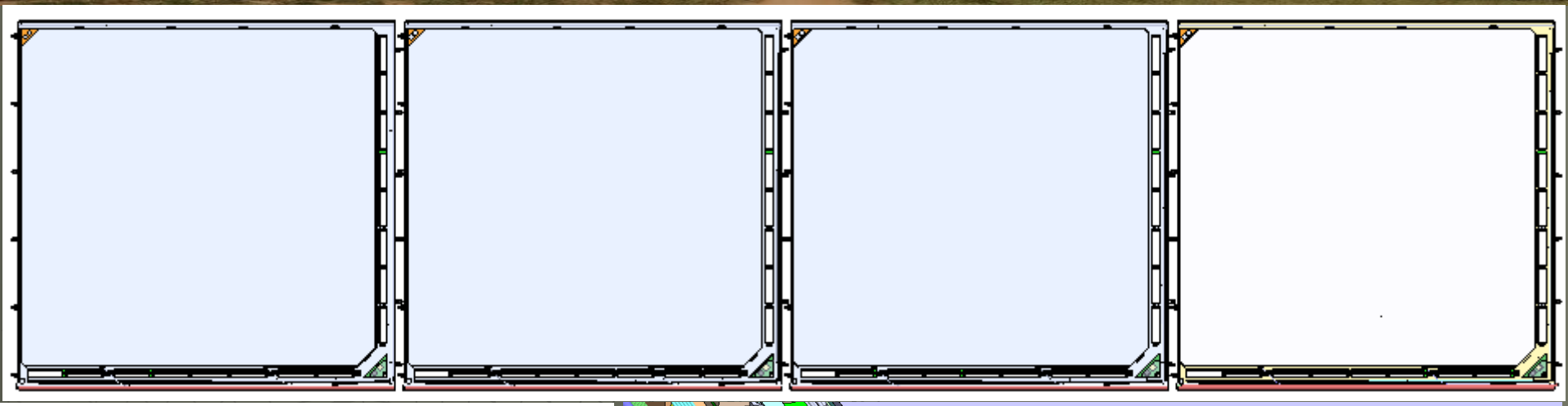
- Multithreaded application that receives Evt and Mon data that is pushed from FrontEnd over dedicated TCP streams
- Keeps alive one TCP sockets stream for each FE-DAQ (RPC), it us estimated that one 12 core Linux server will suffice for 2000 of FEDAQ.
- One thread reads the GlobalTrrigger (UDP) packets and keeps the info in circular list, thereby automatically enforcing a timeout window

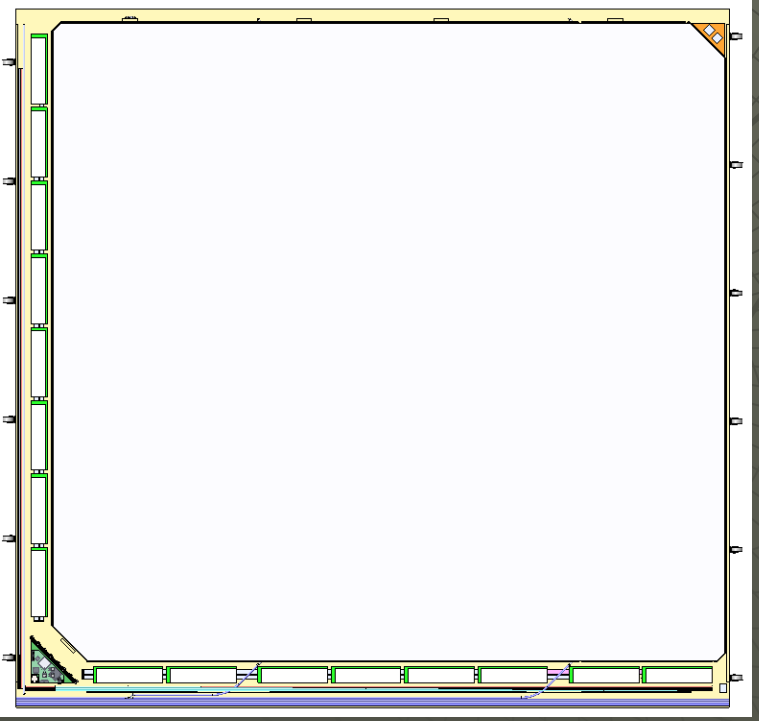


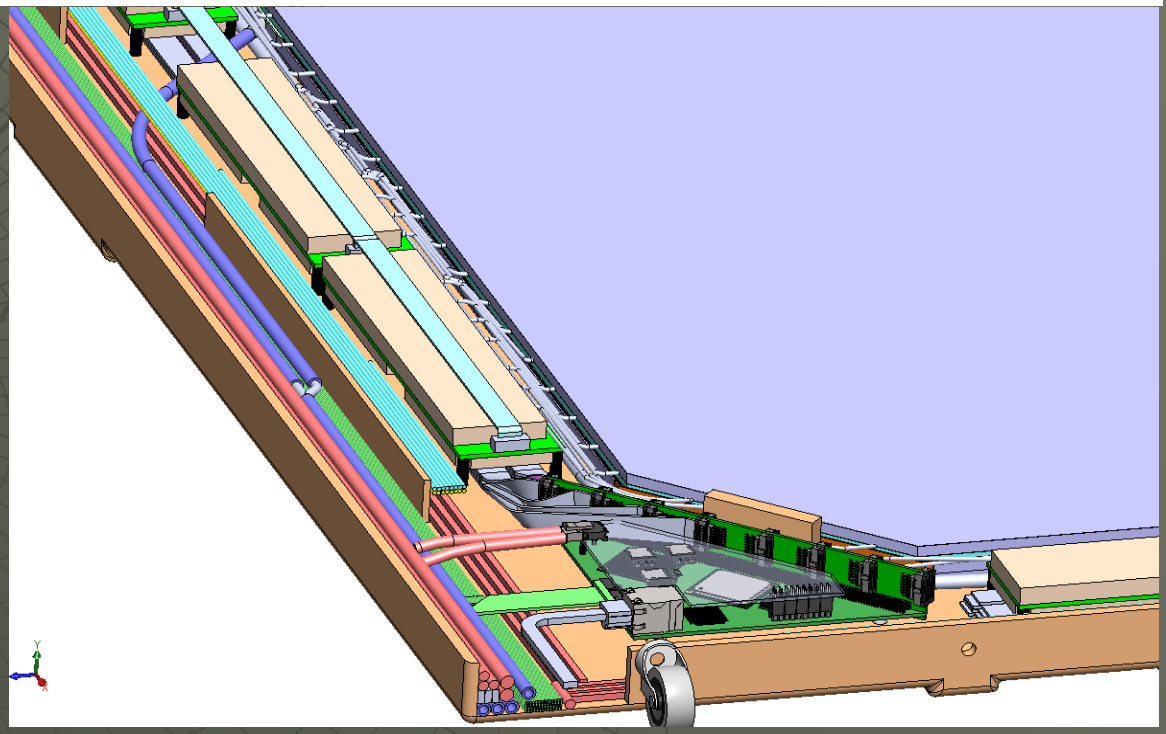
EventBuilder (BARC-ED Group)



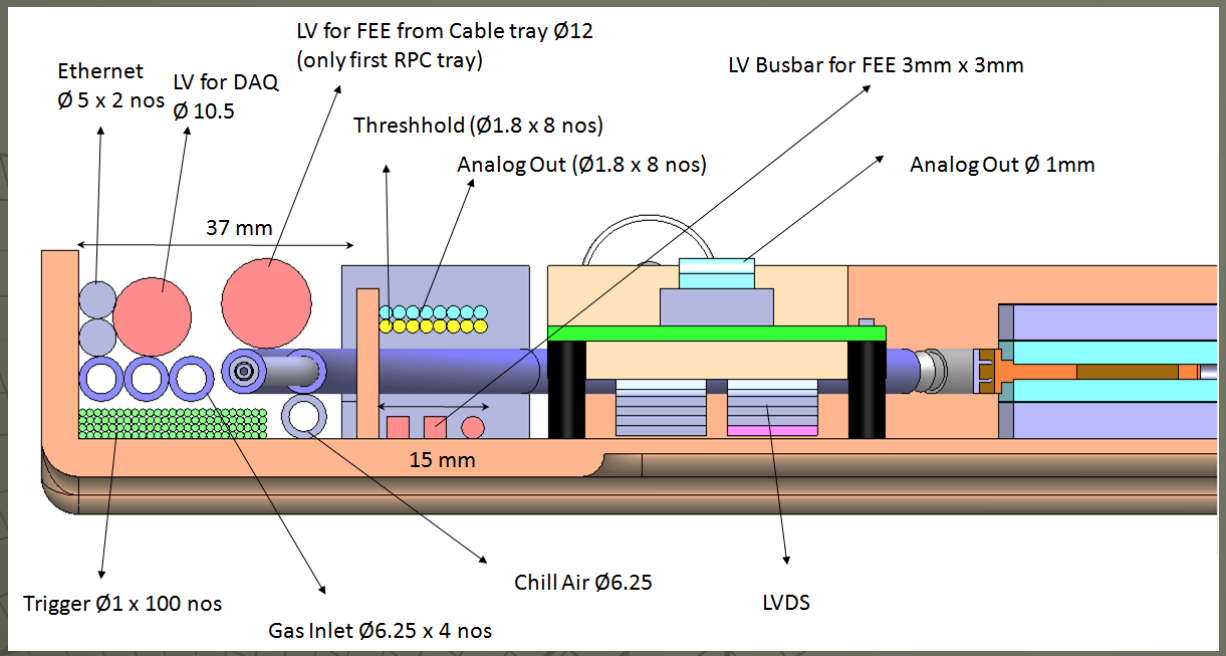
Integration of electronics in RPC

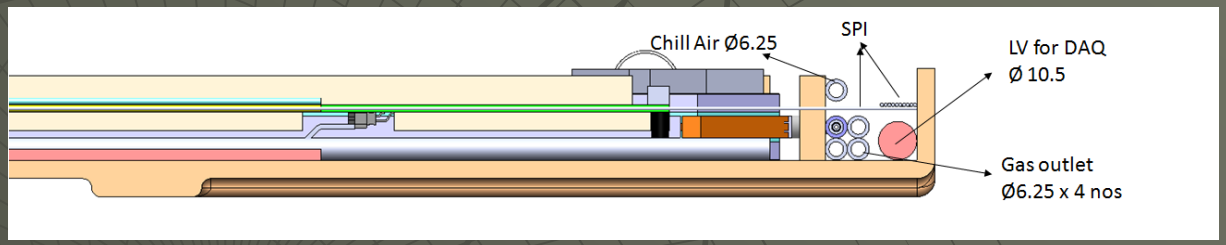


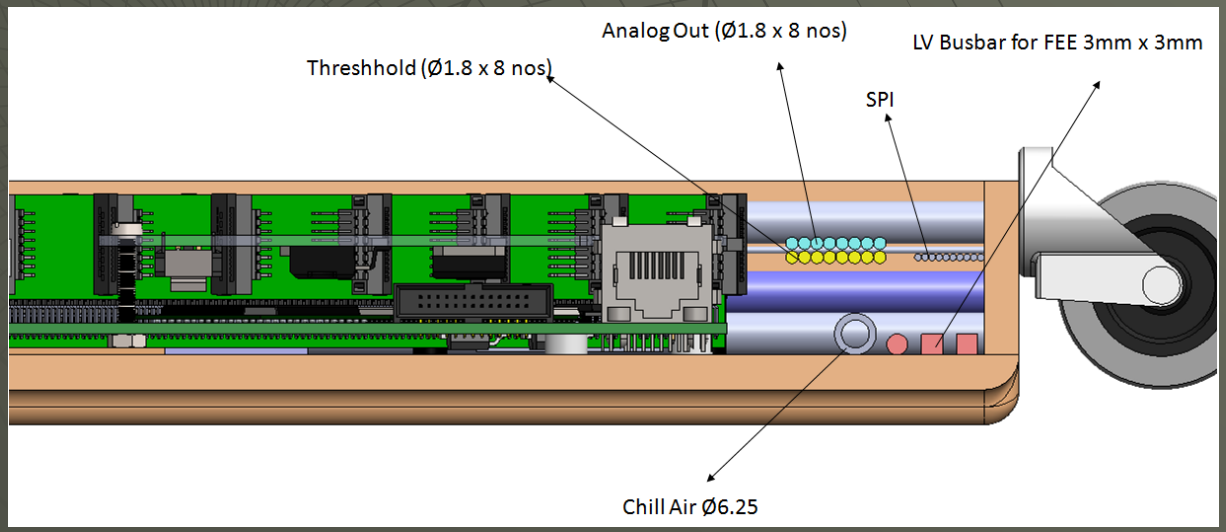




Side views of the RPC tray







Status of ICAL electronics

- Analog Front End ASICs developed, boards fabricated and tested on RPC test stands. Ready for production.
- Digital Front End board designed, fabricated and tested on RPC test stand stands. Ready for production. Firmware, processor software, network protocols, data structures are all designed. Design validated on two target FPGAs.
- ICAL TDC ASIC. Design of the third and final version ready for submission.
- Global services and calibration module designed, currently under production.
- Trigger scheme validated, most of the boards already produced. To be integrated and tested in the detector stacks.
- High voltage module designed, produced, tested on RPC, will go for production soon.
- Backend DAQ hardware configured, to be purchased.
- Data concentrator and event builder software developed, under testing and bench marking.
- Data quality monitors, data storage solutions under development, will be frozen soon.
- Integration of front-end electronics on the detector tray is being tackled and modelled.
- ….. so essentially waiting ☹


Thank you for your attention

BACKUP SLIDES

Dead time of FE software

100 MHz

Event Data Processing Scheme Test with Measurement of event loss percentage at various rates(1 KHz to 10 KHz Random triggers) with Fixed & variable Event size

Random Triggers Mean Freq (KHz)	Event Triggers Sent (millions)	16 TDC 600 bytes		10 TDC 408 bytes		5 TDC 248 bytes		1 TDC 120 Bytes		Random TDC Data size	
		Events Rcvd	Loss (%)	Events Rcvd	Loss (%)	Events Rcvd	Loss (%)	Events Rcvd	Loss (%)	Events Rcvd	Loss (%)
5	3	2516125	16.2	2999029	0.1	2999931	0.002	2999971	29 eves	2852114	4.92
10.1	3	1268117	57.8	1886713	37.2	2999516	0.016	2999951	49 eves	1937811	35.5

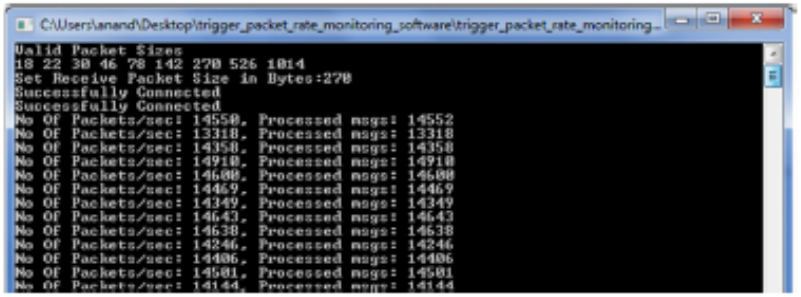
Random Triggers Mean Freq (KHz)	Event Triggers Sent (millions)	16 TDC 600 bytes -52		Random TDC Data size(8 – 548)	
		Events Rcvd	Loss (%)	Events Rcvd	Loss (%)
5	3	2720117	9.3	2883408	3.8
10.1	3	1382499	53.9	2053878	31.5

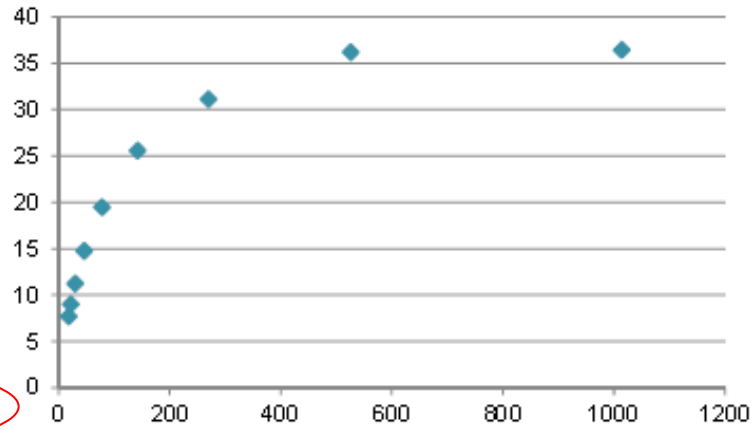
NOTE:
1. H/W FIFO used and
2. Wiznet write Cycle time 360ns and 3. Gate opening delay of 5 us

Hardware based Wiznet

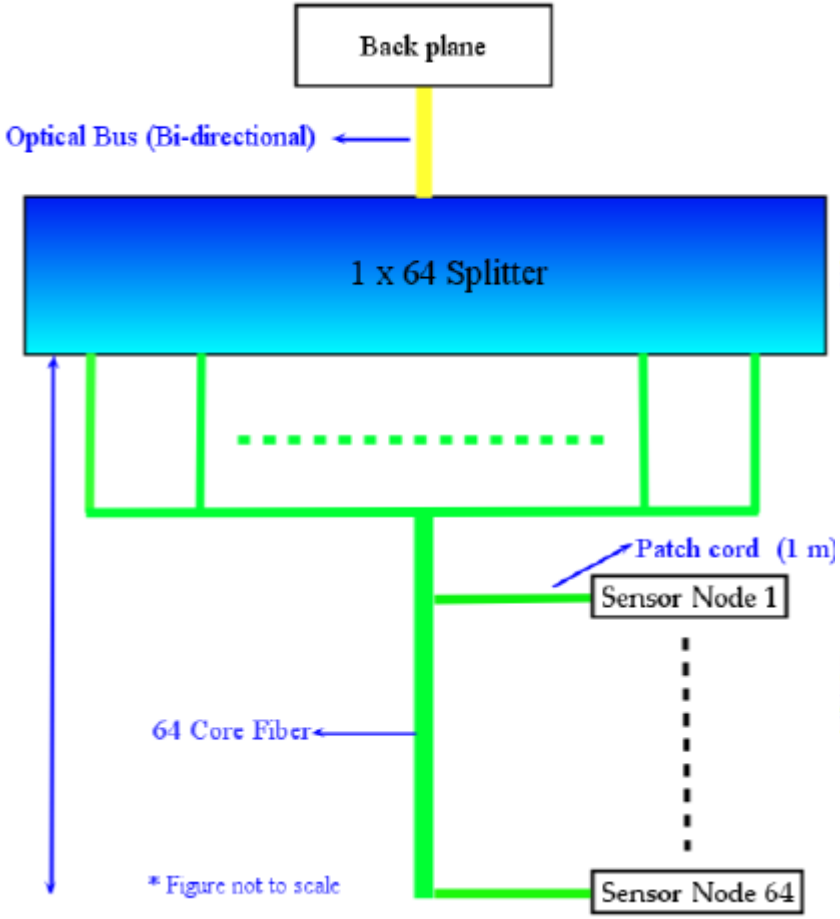
CAM testing

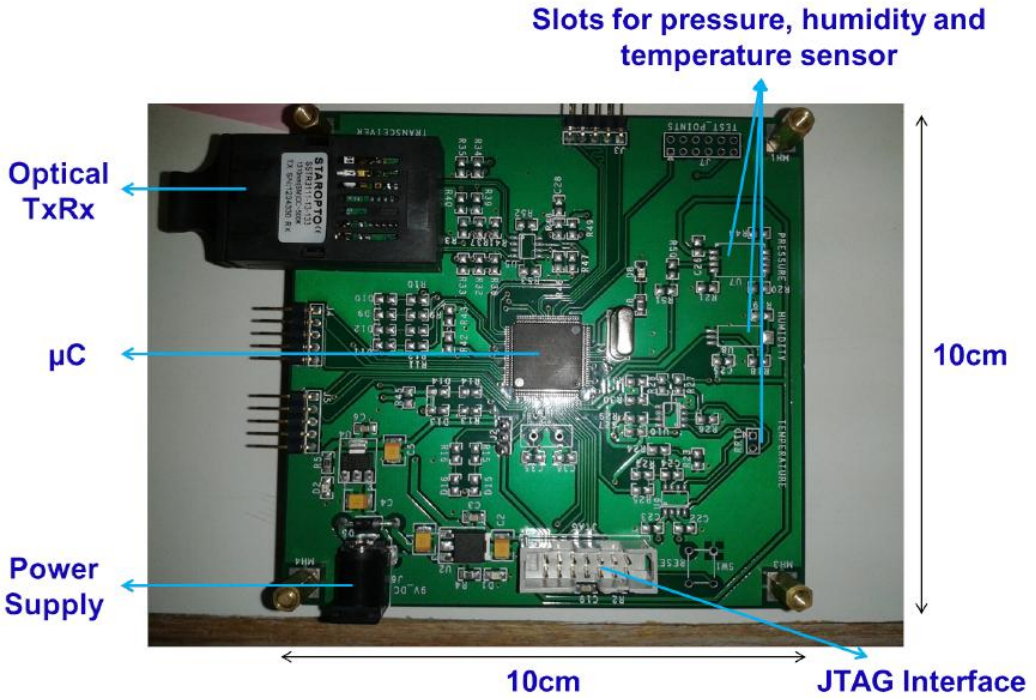
Packet (bytes)	Packet Rate (Hz)	Date Through put MB/s
18	53450	7.6968
22	51140	9.00064
30	46800	11.232
46	40100	14.7568
78	31200	19.4688
142	22500	25.56
270	14400	31.104
526	8600	36.1888
1014	4490	36.42288



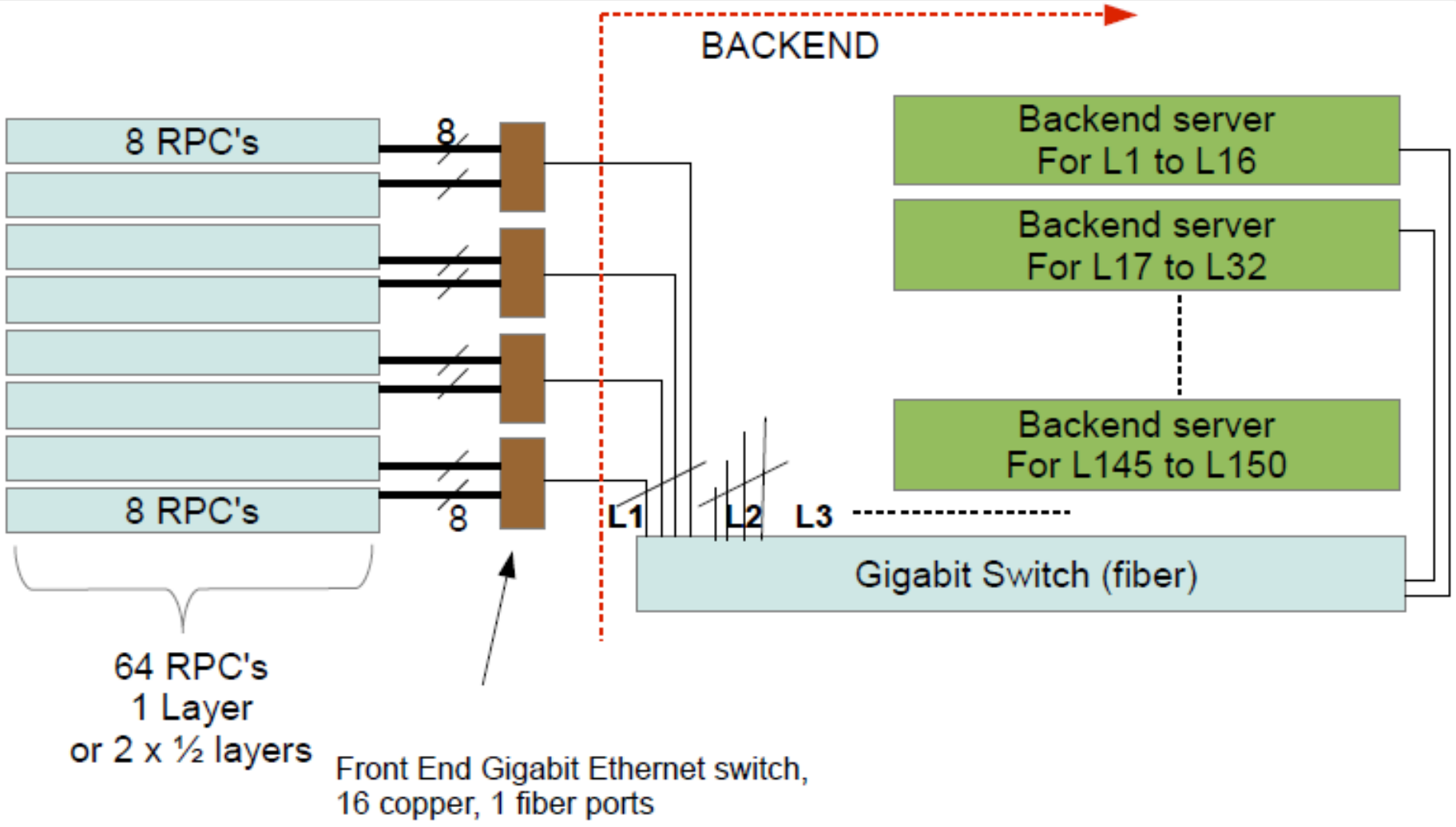


Passive Star Optical Networks

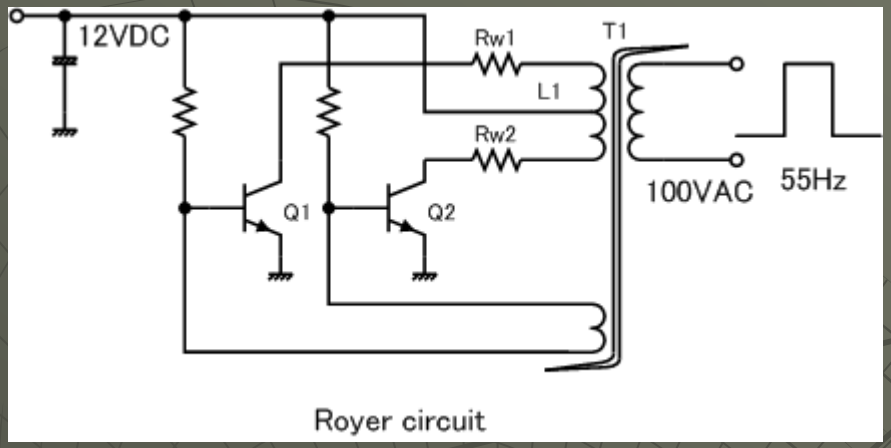




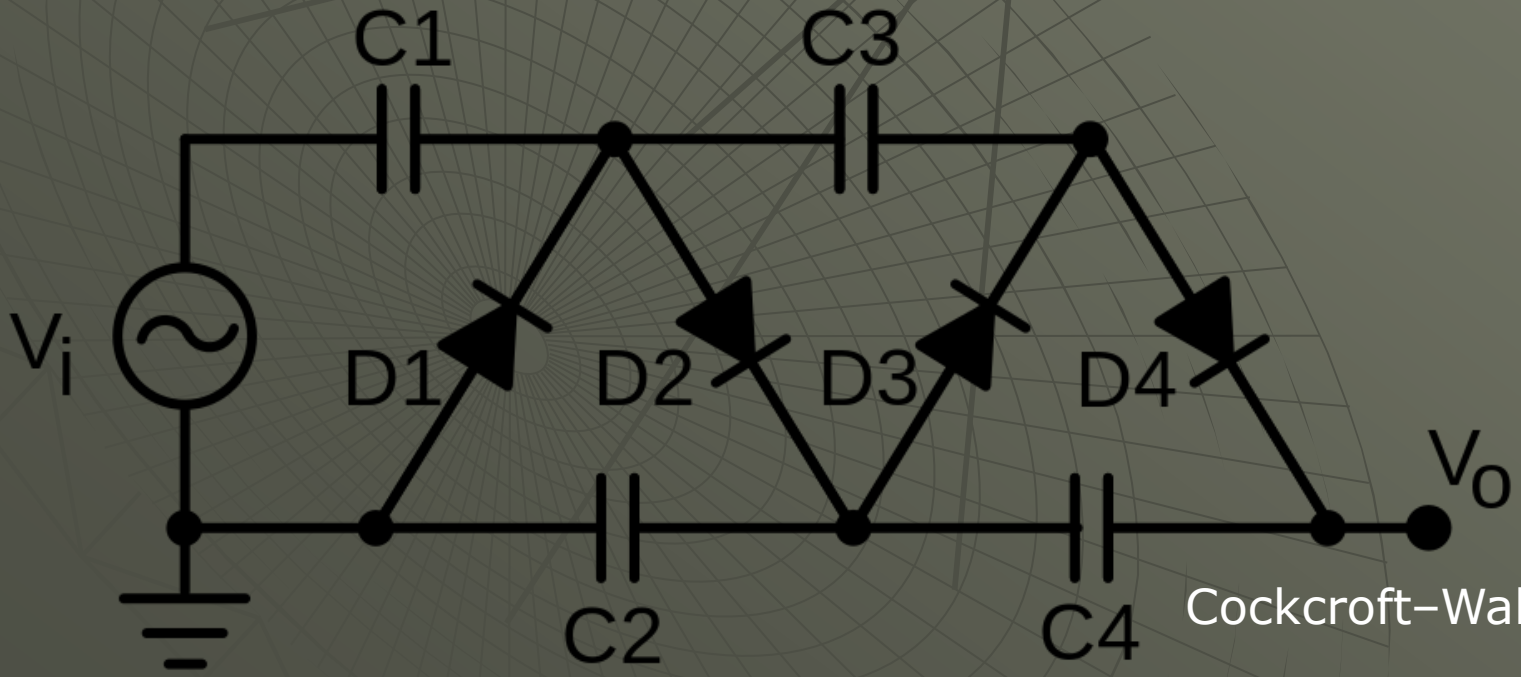
Data network schematic



High Voltage power supply



Royer circuit



Cockcroft–Walton generator