HEP JOURNAL CLUB

Trigger and DAQ for HEP Experiments

A brief introduction : Concepts and Terminologies

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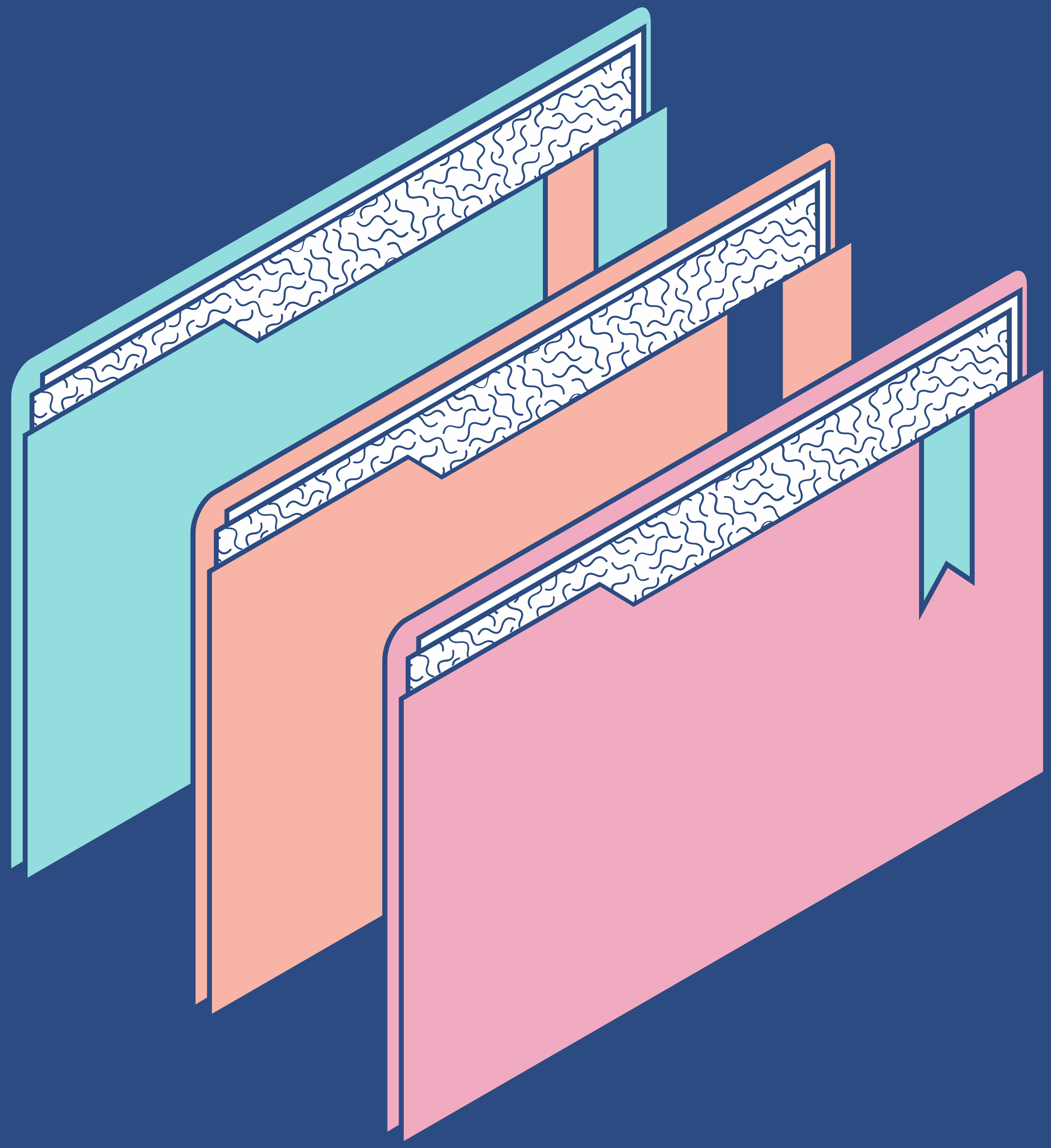
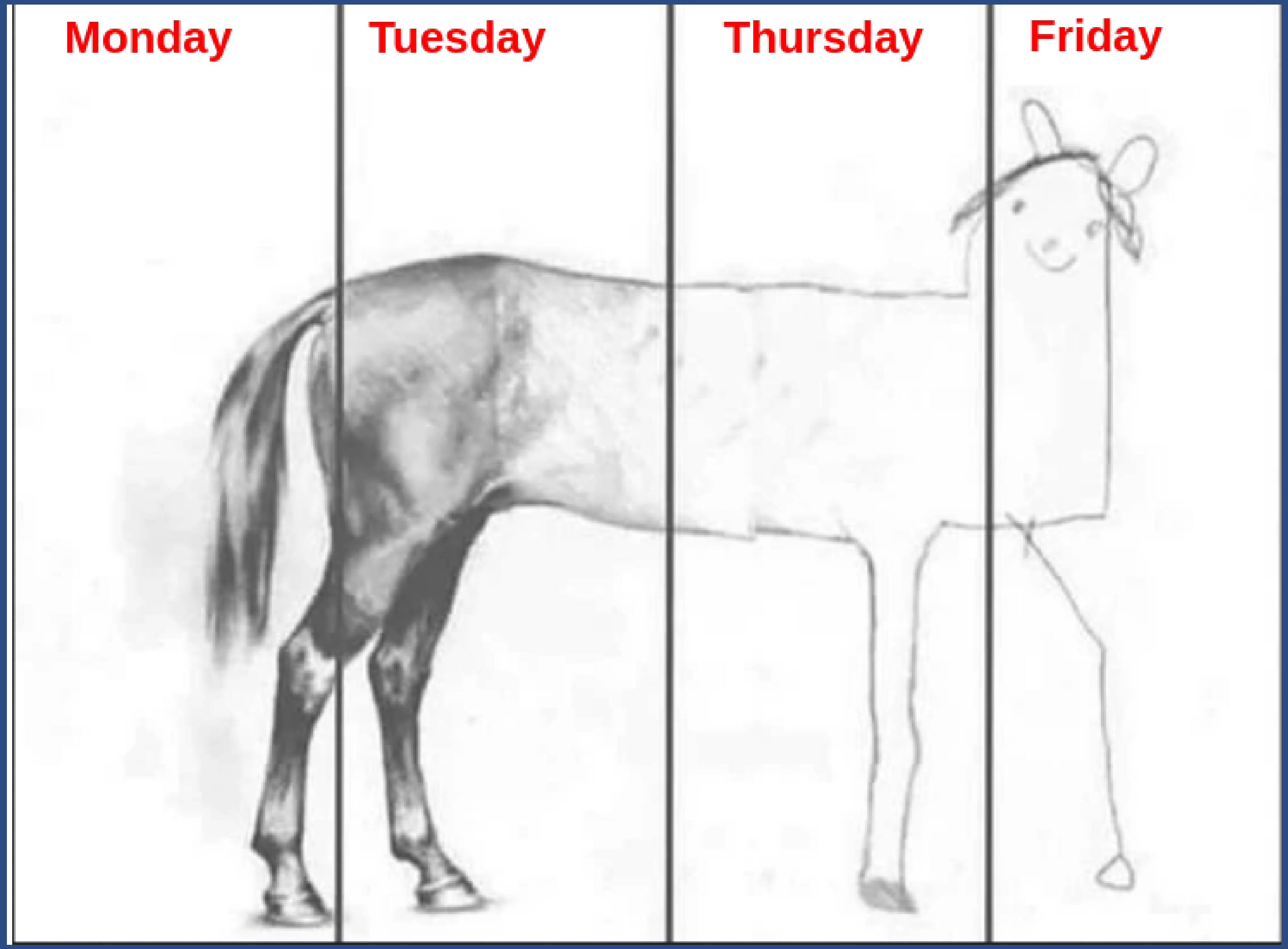


Agenda

KEY TOPICS DISCUSSED IN THIS PRESENTATION

- What is DAQ , importance , from physics to Taking the relevant data
- History bubble chamber girls / Spark chambers / CG17
- Common instruments used
  - Digitization
  - ADC / TDC / Comparators / Logic Gates
  - Delay lines / Ring Buffer / Memory
  - Transfer protocols
  - Technological limiatations limitations
  - Typical data handling rates
  - Deadtime and DAQ Preassure
- DQM :
  - Concepts
  - Anomaly detection , make sum bad joke on ML , refer to Mintus commads
- Collider example
  - Focus on CMS / Belle as proxy
  - Gets time will do Cosmic ray some other time


Monday
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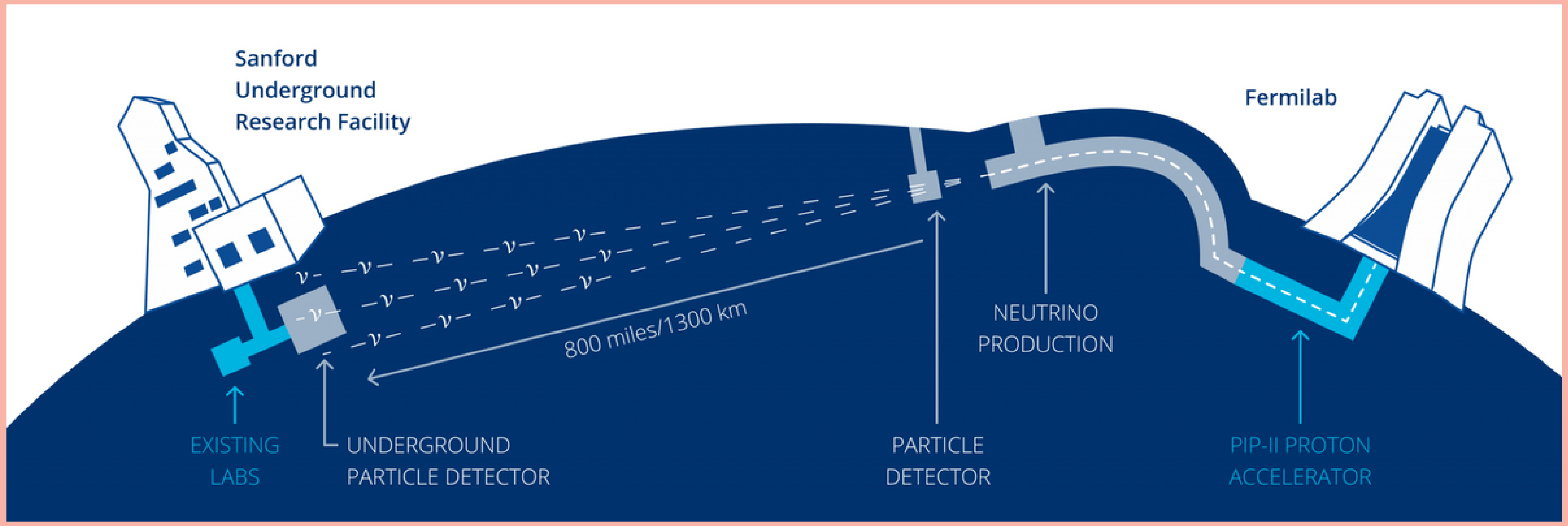
HEP Experiments

PLANNING OF THE EXPERIMENT

Physics Goal :

- Search for a Dark matter candidate
- Identify the mass ordering of neutrinos
- Find Higgs
- Precision Measurements



Design the Detector Concept

- Conceptualization of the detector components
  - Momentum measurements ? : tracker
- Understanding what signatures to search for

Data Aquisition Considerations

- Estimation of detector occupancy
  - Estimation of Data Flow Rates
    - Affordable Dead time ?
    - *Affordable Event Size* ?
    - Storage Limitations ?

CMS Experiments

SOME CONSIDERATIONS

Physics goal @LHC

- **Precision Electroweak measurements**
    - **precise momentum measurement and vertexing of charged particles**
    - **Excellent Calorimetry**

Detector Concept @ CMS :

- **n - Si Tracker layers at high 4T**
    - CMS Pixel Detector

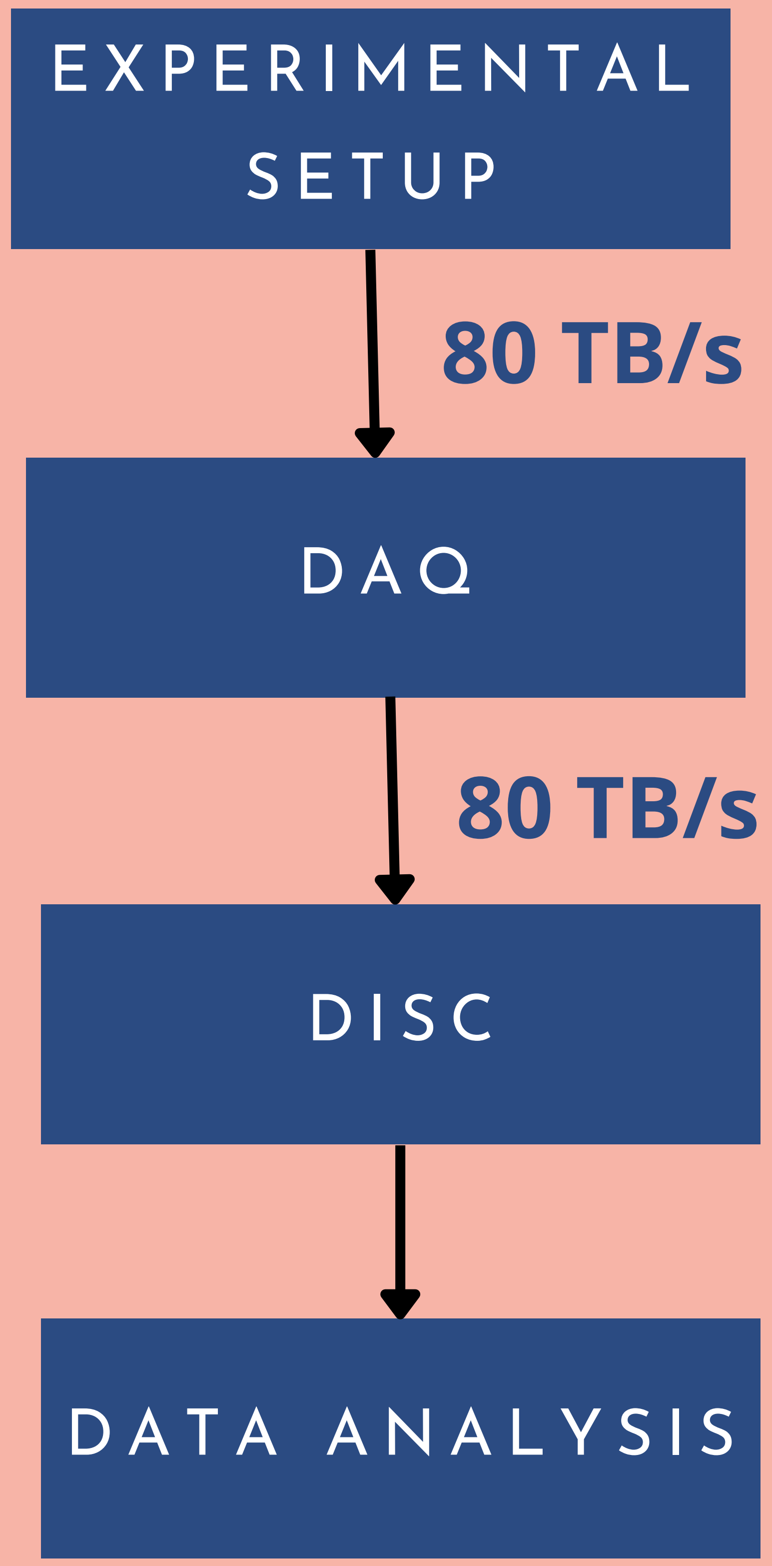
Challenge

- 77 Million channel
    - Each says Hit/Not Hit
    - **--> > 1 Mb in a single read out at 1% occupancy ‼**

LHC Experiments

SOME CONSIDERATIONS

- Bunch crossing rate: 40MHz
  - front-end electronics ready every 25 nano-sec.
- Luminosity at IP 1e34 /cm2/sec
  - p-p cross section : 80 x 1e-27 cm2
  - Rate --> 0.8 GHz !!
- A single event is approx 1.0 MB
  - ~800 TB/s data-flow for readout
  - realistically its approx 80 TB/s



Challenge : Store and process the data for achieving the physics goals

- **Is all of this 80 TB required for achiving the physics goal ?**
- **More data stored --> more data to analyze/ more network+compute usage**
  - **Global Warming !**

DAQ : Rates and Deadtime

- Dead time The time lost in DAQ when Read out is not possible
- We can control the trigger rates by adjusting the logic
- We want to maximize the ratio of R_{out} / R_{in}

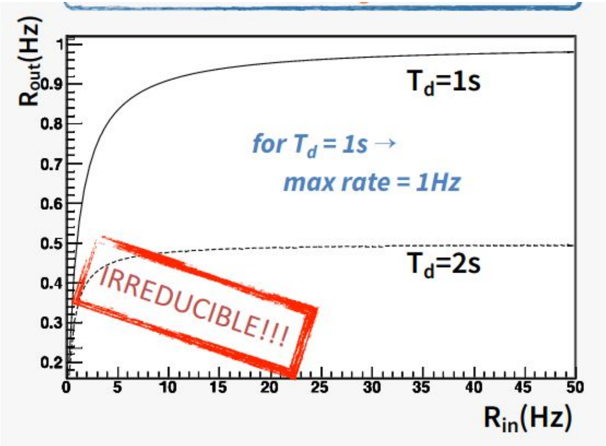
R_{in} = Trigger rate (average)
R_{out} = Readout rate
T_d = processing time of one event

  - Read Out Rate from Trigger Rate

$$\text{Time DAQ is supposed to be busy} = R_{in} * T_d$$
$$\text{Farction of Events Lost} = R_{out} * T_d$$

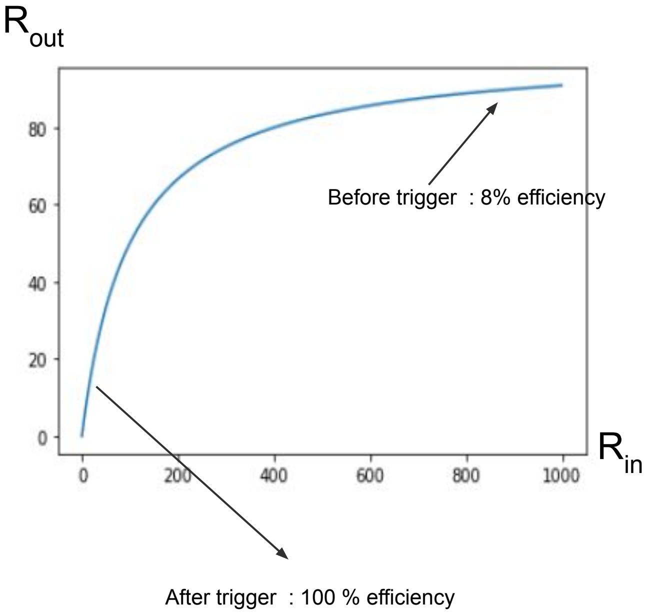
$$\text{Farction of Events Read} = (1 - R_{out} * T_d)$$
$$\rightarrow R_{out} = (1 - R_{out} * T_d) * R_{in}$$

$$\frac{R_{out}}{R_{in}} = \frac{1}{1 + R_{in} * T_d}$$



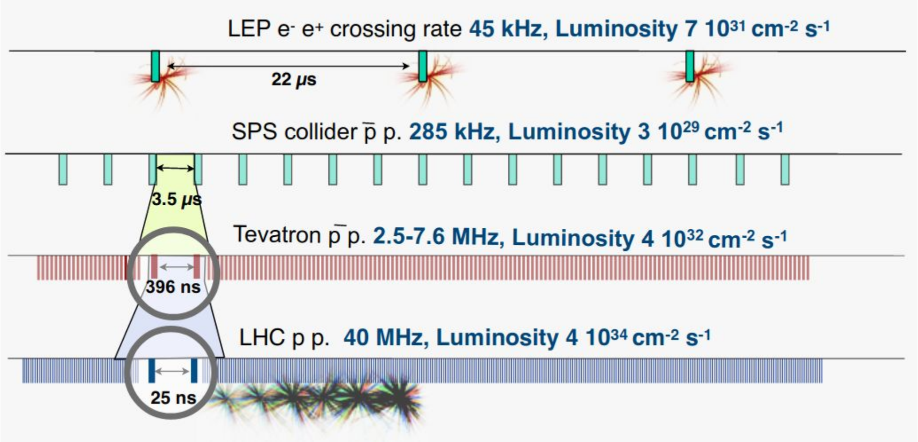
Understanding the Need for trigger from *deadtime*

- Assume there is no trigger logic in place
  - We **try** to readout all events
- Rate of Events = R_{In} (= 1000 Hz)
- Rate of the physics process we want to study
  - 10 Hz ($R_{in}^{physics}$ = 10 Hz)
  - What is the Efficiency we expect ??
    - $$\frac{R_{out}}{R_{in}} = \frac{1}{1 + R_{in} * T_d}$$



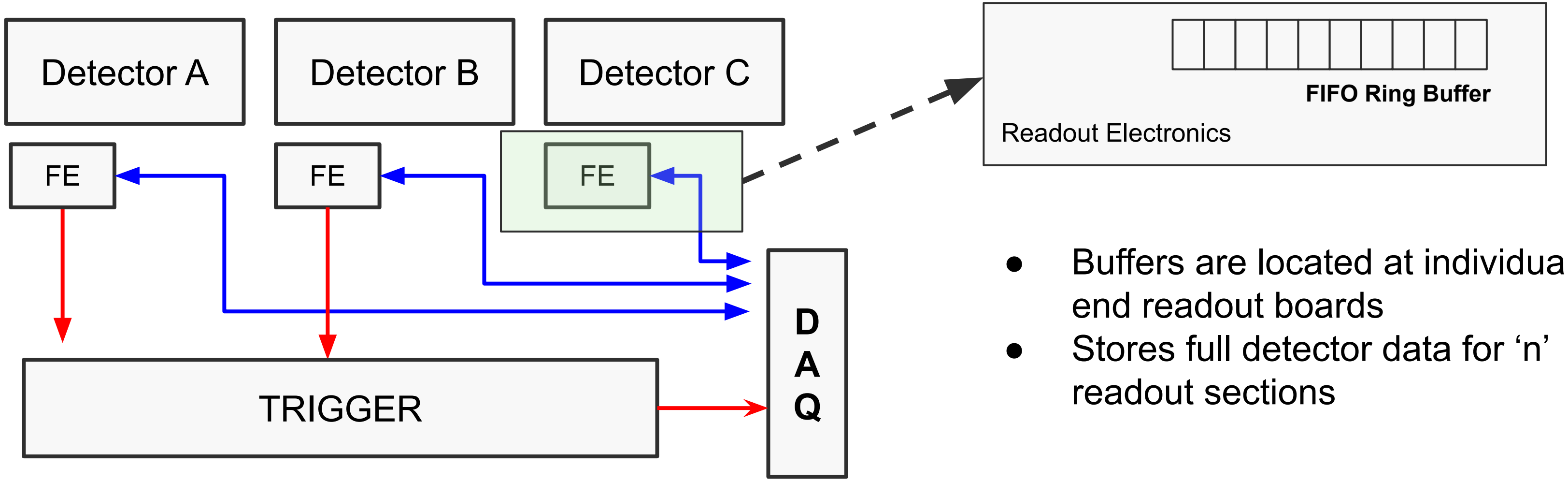
DAQ With Buffers

Challenge : Huge event rates ⇒ Available processing time ~ 50 ns



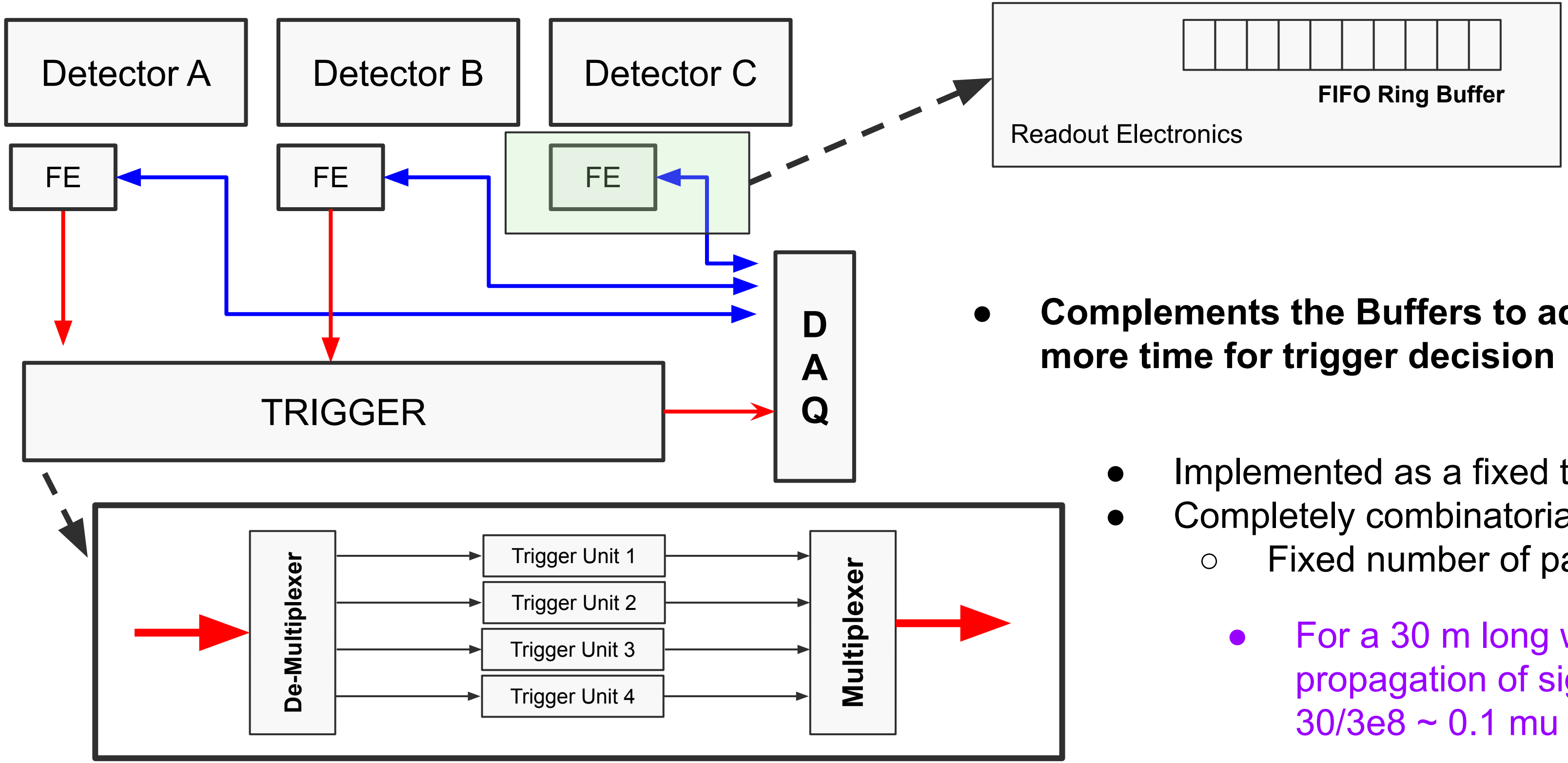
- Temporarily store data in memory while trigger decision is made
  - First in First out : FIFO
    - Ring buffer
  - Require very high speed memory
    - Costly [very costly]
  - CMS has 128 Bx buffer
    - 25 ns x 128 ⇒ 3.2 mu sec

DAQ With Buffers



- Buffers are located at individual front end readout boards
- Stores full detector data for ‘n’ readout sections

Buffers and Time Multiplexed Triggers

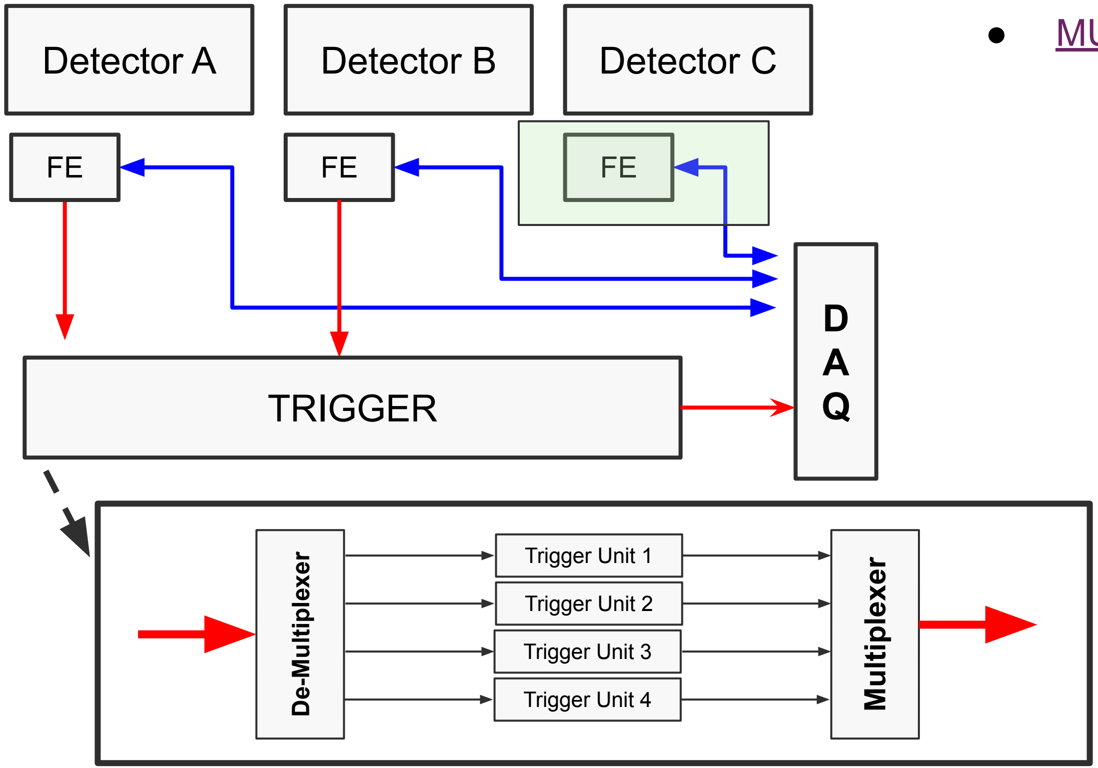


- **Complements the Buffers to achieve more time for trigger decision**

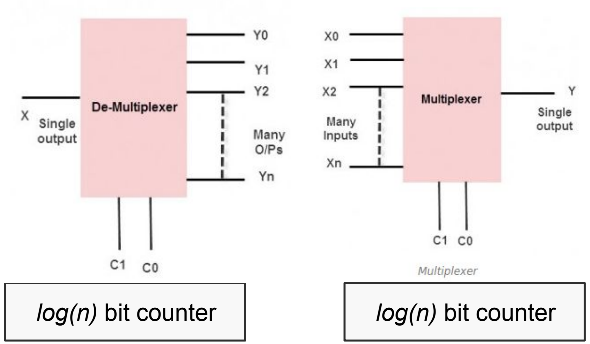
- Implemented as a fixed time setup
- Completely combinatorial circuits
  - Fixed number of particle

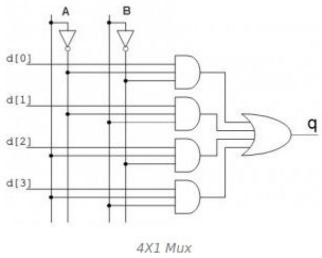
- For a 30 m long wire t of propagation of signal : 30/3e8 ~ 0.1 mu s

Buffers and Time Multiplexing



- MUX and DeMUX





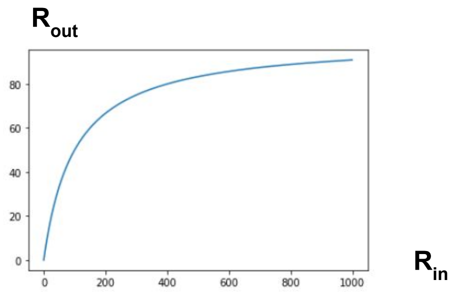
Deadtime ?

- If buffer is long enough , the trigger decision is available by the time the buffer gets filled up
  - So is there no dead time possible now ?

Deadtime and DAQ Backpressure

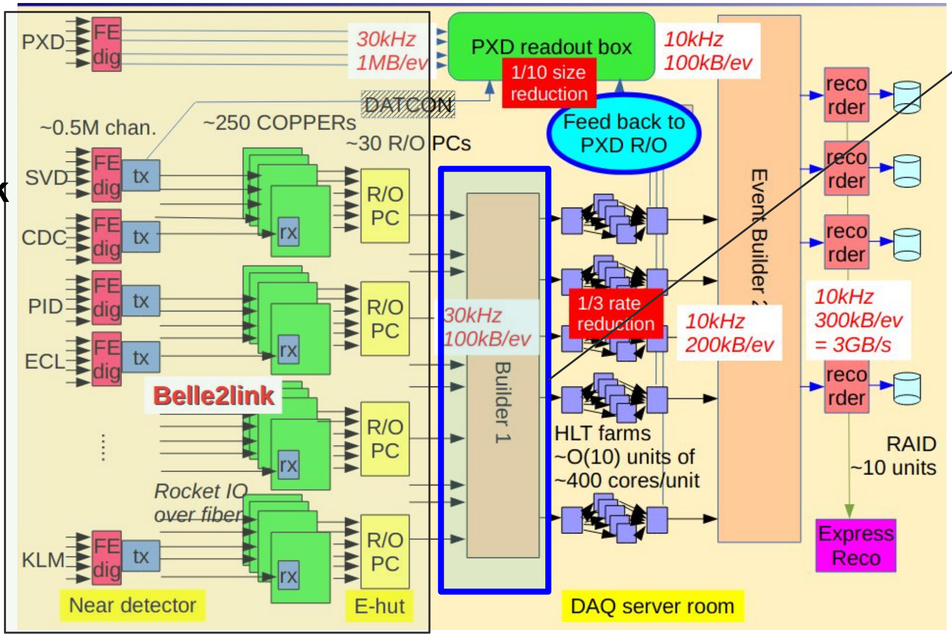
- If buffer is long enough , the trigger decision is available by the time the buffer gets filled up
  - So is there no dead time possible now ?

- Capped by the buffer to Network readout bandwidth
  - 100 GB/s with 1 MB per event : ~ 10 mu sec of readout from buffer
  - As the next positive trigger decision comes , the event might not be there in the ring buffer
    - **DAQ Backpressure**
      - **Inability to sustain the dataflow**



Event Re-Building and Storage

Trigger Block



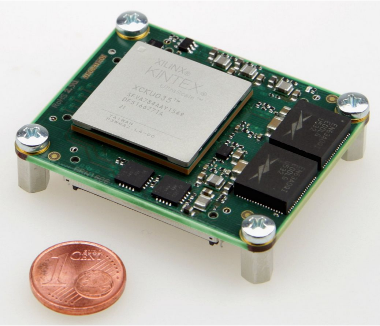
- Collects the information into a single object
  - Merges the ***headers and messages*** to an ***Event***
- Custom Hardware boards designed
  - For very high throughput

Technologies Used : Readouts and Trigger

- Depending on the detector , readout devices vary
  - Radiation hard electronics when sitting very close to the IP
    - ***Costly***

- Generic devices used at front end
  - qADCs : Analog to digital converters [Calorimeter]
  - TDCs : precision timing measurements [Muon chambers / trackers]
  - Digitizers

Technologies Used : Readouts and Trigger



- Depending on the detector , readout devices vary
  - Radiation hard electronics when sitting very close to the IP
    - ***Costly***
    - ***Custom ASICS***
- Trigger logics are implemented FPGAs
  - FPGAs are configurable electric boards
    - You can code your logic in the language of your choice
    - Convert it into a circuit : Tools in place to do this
    - FPGA provides an array of gates that can be connected based on choice
      - Actually a bit more complex than this : Implemented as LUTs
  - FPGA market a monopoly by Xilinx [bought by AMD now] : so things are costly
    - Intel also entering the field now
- Implementation of CPUs inside FPGAs make them much more versatile
  - **SoCs : System on Chip**

Single Bit Upsets

Technologies Used : Storage

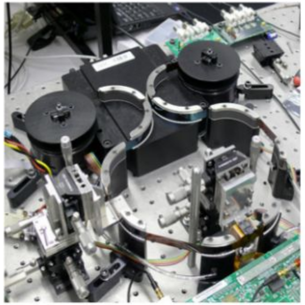
- After DAQ (+ Trigger) the data is copied to the tape for permanent storage
- Tapes : Archival Storage for Scientific Computing

Comparing tape and disk

	Tape	Disk
Data transfer rate	400 Mb/s	200 Mb/s
Positioning type	**Fast Sequential Access**	**Fast Random Access**
Average positioning time	30 seconds (610 m @ 12 m/s)	5 milliseconds
Latency to first byte	A few minutes	5–10 milliseconds

Advantages of Tape : Reliability and Data Security

- Two heads are better than one : read after write verification
- No data loss if a drive fails
- Immutable files
- Air-gap security
- Long media lifetime (30+ years)



Multi Level trigger system

- For very large Data rates , a hardware trigger is not enough
  - For looking for complex signatures
  - Cross detector information
- Usually a CPU Farm sits over the hardware trigger layer that can do a full event reconstruction , or do a quick ***quick physics analysis***.
- For CMS the 100 GB/s from the hardware to ~ 10 GB/s of good physics data

- Some exotic developments you can read on
  - Triggerless DAQ for Alice Experiment
  - LHCb trigger upgrade that uses GPUs to do full HLT on all readout events [TDR]

Organization of Trigger bandwidth

- Bandwidths allotted to each physics searches based on the global strategy of the experiment
  - Would charge change time to time and new deviations comes popping up
- Generaal Calibration and Monitoring triggers
- Analysis specific triggers
- Trigger bandwidth for physics groups

Some Readings

- **Synchronous and Asynchronous trigger**
- Grapes example
    - An Advanced Triggerless Data Acquisition System for GRAPES-3 Muon Detector
- Event triggering in the IceCube data acquisition system