CMS HCAL Phase-1 Upgrade

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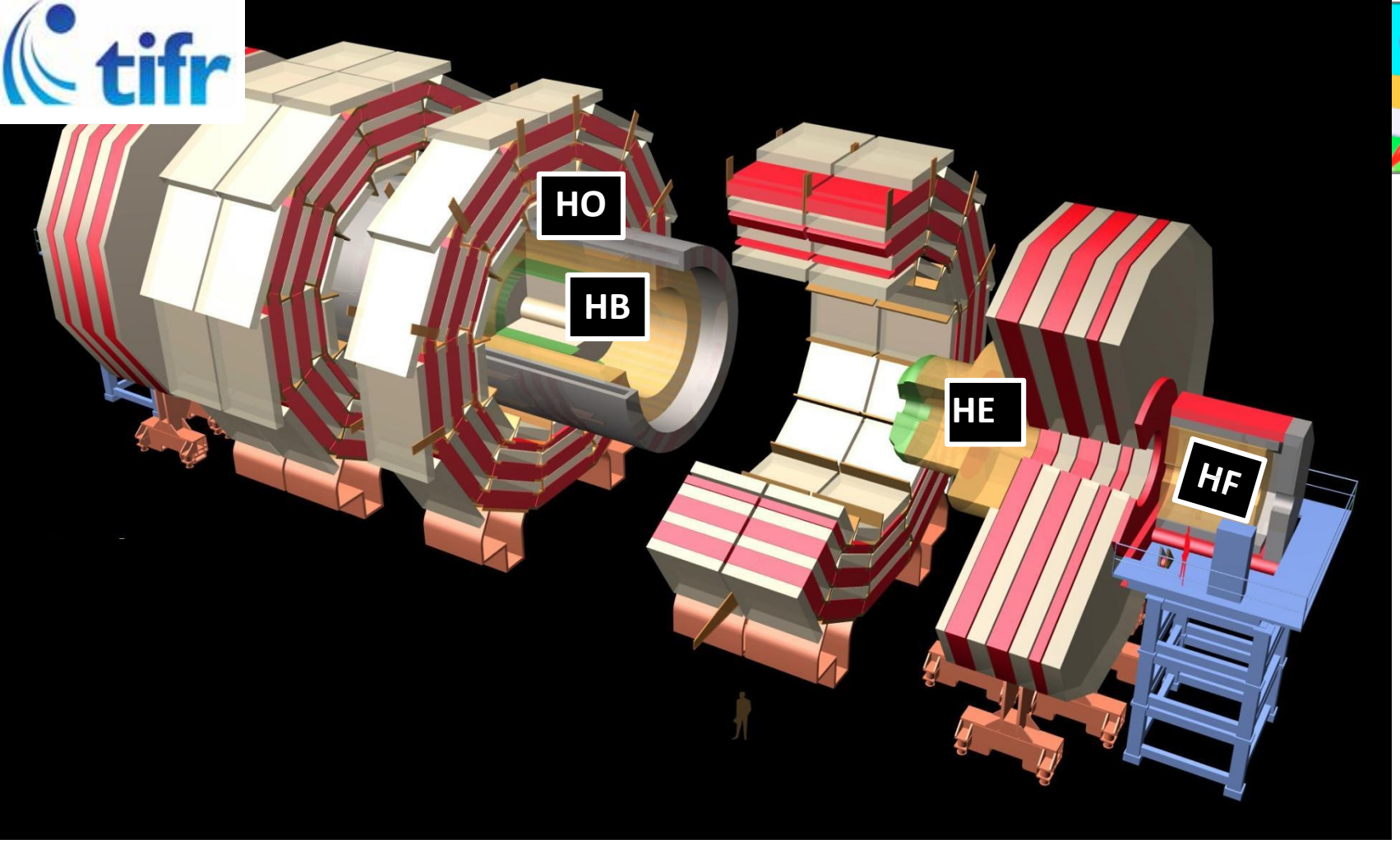


HCAL HB and HE Upgrade of FEE-Current focus

Review of CMS Hadron Calorimeter

- HCAL starts at R ~ 180 cm and Z~ 400 cm from interaction point.
- Sampling calorimeter providing up to 11 interaction lengths (at eta=0) for hadronically showering particles
- Essentially plastic scintillators with embedded wave-length shifting fibres, interleaved with brass in HE, HB regions → ~72000 tiles
- Light read out with photo detectors: HPD→ Silicon Photomultipliers (SiPM)

Legacy detector with HPDs ~ 10k channels (HB: 2592, HE: 2592, HO: 2160, HF:1728)

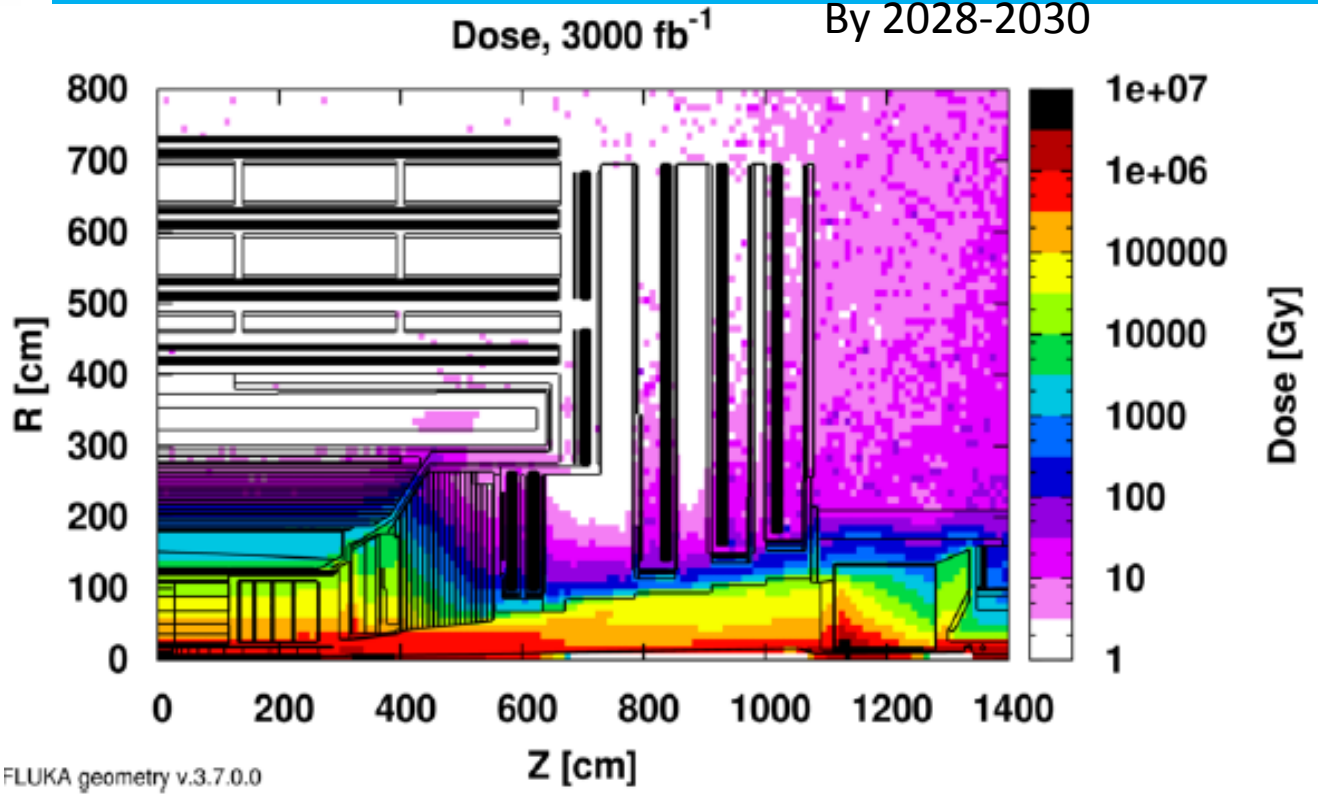
- Performance directly impacts trigger capabilities through measurements of jets, missing transverse energy and other kinematic variables

CMS detector designed in 1990s was not meant for High lumi operation of LHC

Radiation damage suffered by HCAL detector during LHC Run1 is worse than anticipated.

Anticipated does rate at HL-LHC

By 2028-2030



- Light output of scintillator decreases exponentially with the dose received
- Long term exposure to radiation increases leakage current of HPD

➔ physical change in on-detector instrumentation and front-end electronics

Eliminate high amplitude noise and drifting response of HPDs by replacing them with SiPMs

Why Upgrade? For HB/HE/HO

- Early phase of LHC operation revealed considerable radiation damage of HCAL

➔ Mitigation through multiple ways within existing constraints.

➔ Improved photodetectors, new front-end electronics (including TDC) and new back-end electronics (microTCA)

- HCAL electronics upgrade is one of the major phase-I upgrades for CMS

  → Being carried out in a continuous fashion since 2013.

- Font-End electronics(FEE) for Endcap and Barrel regions to be replaced during 2016- 19

  TIFR responsibility spelt out in CMS TDR CERN-LHCC-2012-015.

➔ Improve energy resolution by exploiting finer depth segmentation

- Frontend electronics replacement schedule for HE advanced than originally planned. Installation planned in EYTS of 2016-17

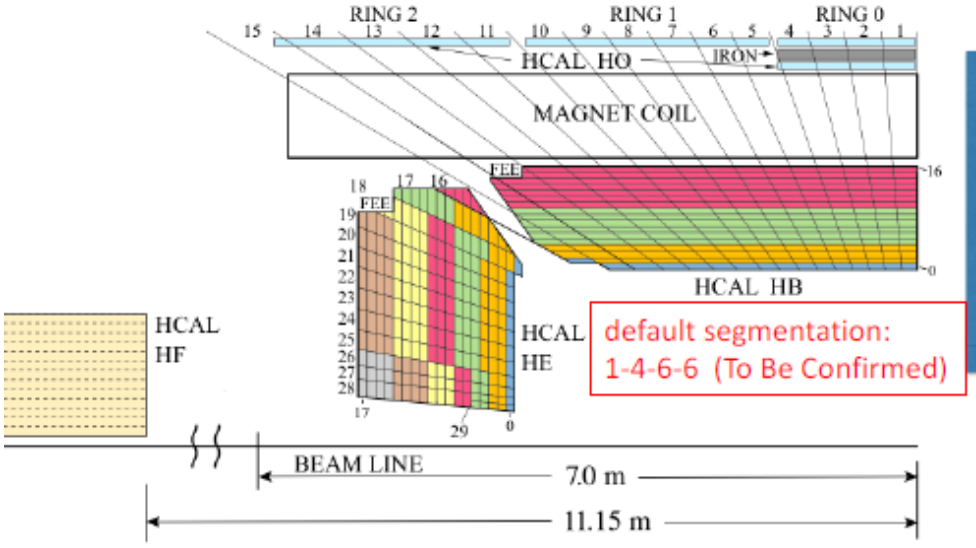
Phase 1 HB Upgrade Features

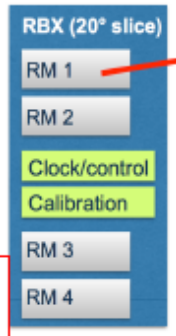
Phase1 upgrade of HB electronics, scheduled for installation during LS2 (2019)

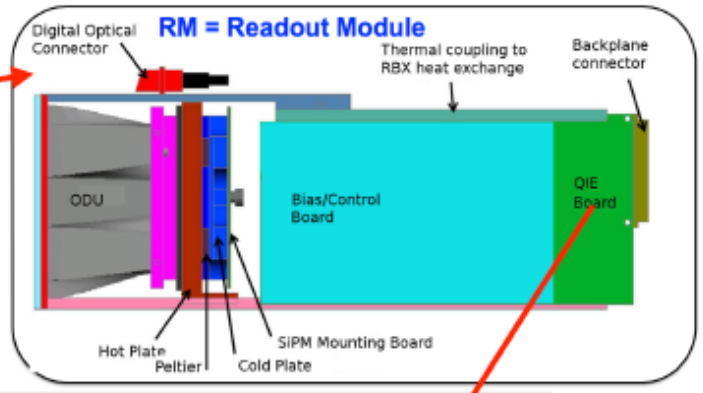
HB Phase1 Photo-detector + Front-End upgrade during LS2:

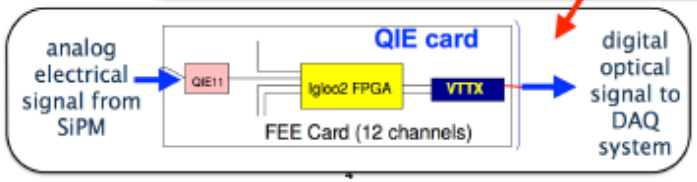
* 144 Readout Modules (SiPMs + QIE11 boards)
* 36 Calibration Units
* 36 Clock-and-Control Modules

Photo-detector	PDE	Gain	Voltage	Performance in B field	channels in 5deg
HPD	12%	2 k	8 kV	good	18 ch
SiPM	35%	350 k	70 V	excellent	64 ch





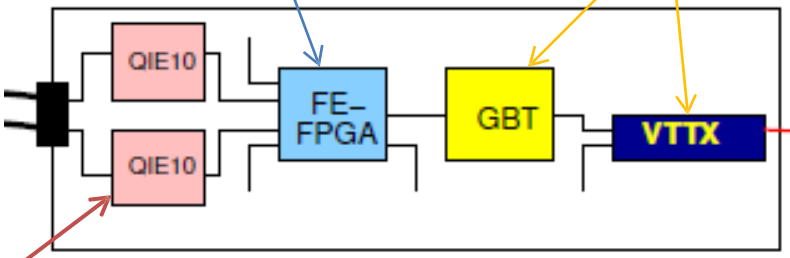




HE/HB Front-End Electronics

Front-End FPGA
- Commercial radiation-tolerant FLASH-based FPGA (ProASIC3E)
- Provides data alignment/formatting
- Pulse-length measurement from discriminator output

4.8 Gbps data link
- CERN Project
- Runs in both FEC and 8b10b modes
- Existing multimode fiber plant capable for 4.8 Gbps data transfer



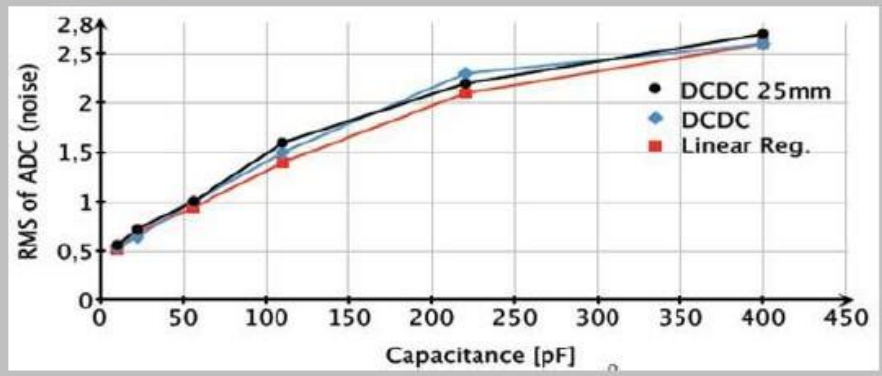
FEE Card (24 channels)

Link Status
- Full GBPTX ASIC sent for fab Aug 2012
- Other link parts complete, production beginning 2013

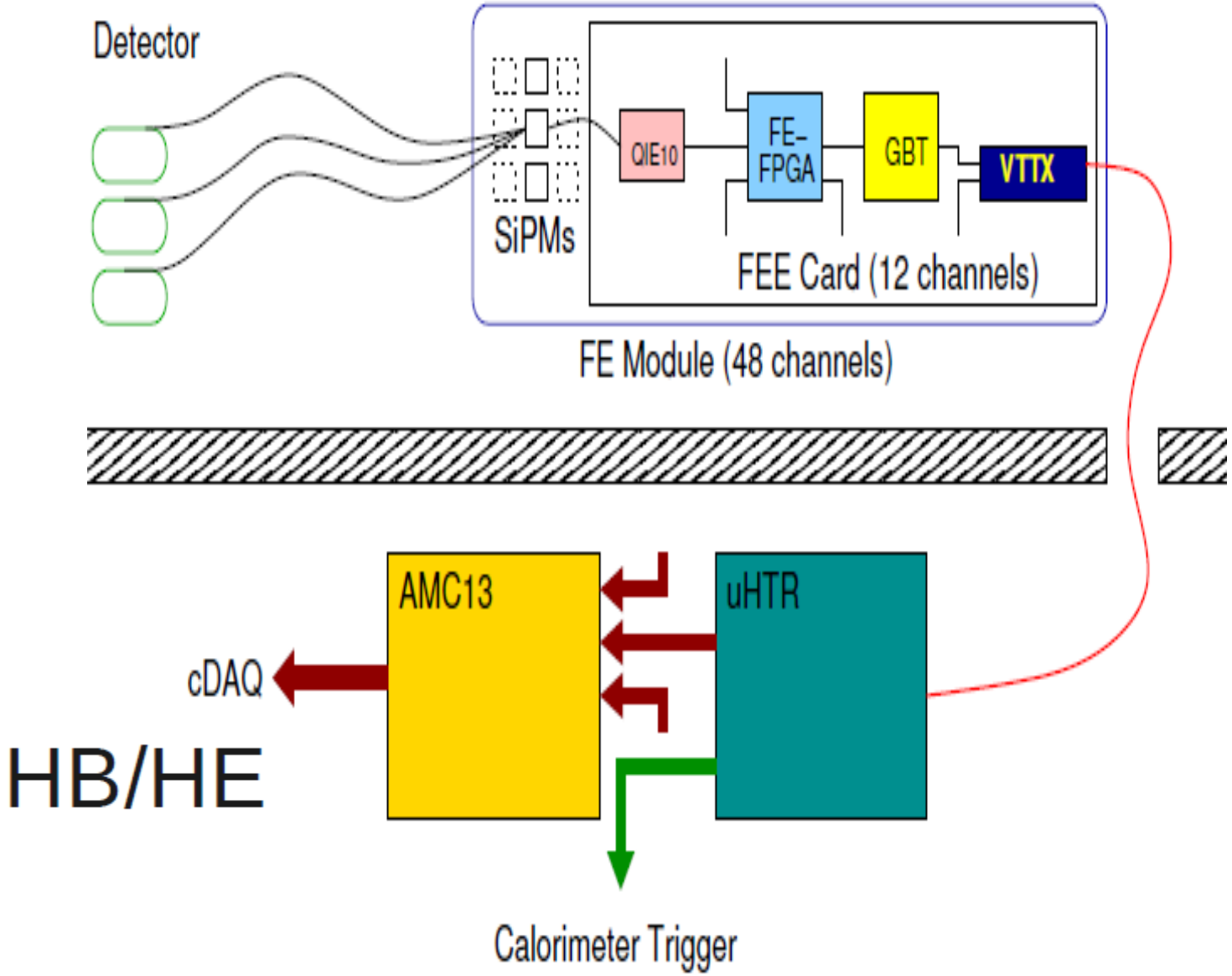
Charge-Integrating ADC
- Dynamic range of 10^5 encoded into piecewise-linear 8-bit code
- TDC capability (500 ps resolution)
- Built-in pulse-injection
- 0.35 µm SiGe AMS process

QIE10 Status
- ADC fully demonstrated
- Full HF version with TDC to be submitted in November

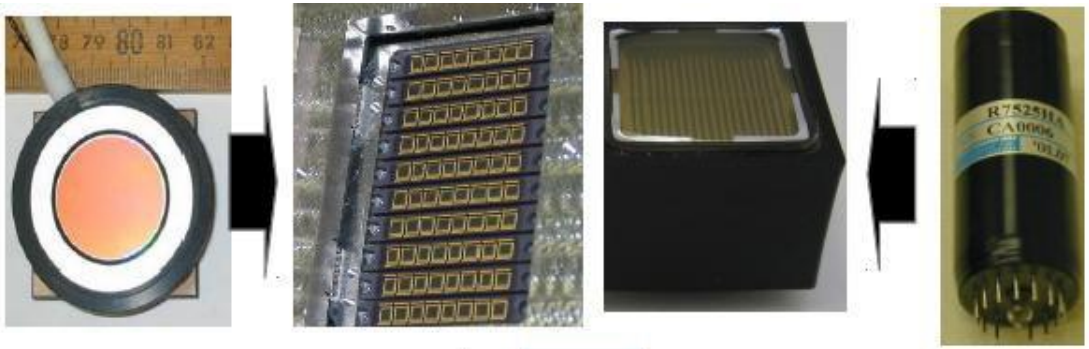
DC/DC power converters based on CERN design

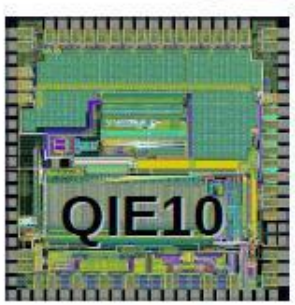


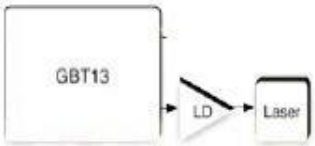
Upgrade in a Nutshell



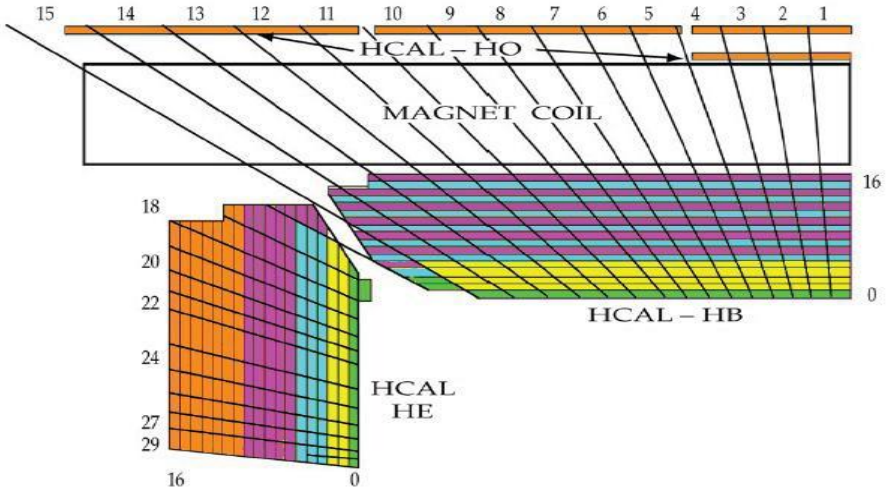
Upgrade in a Nutshell







- Main Idea
  - Replace phototransducers to reduce noise and improve performance
  - Take advantage of new technologies to increase granularity (PFlow), add TDC information (pileup), etc.
  - Use as much common components as possible
  - Back-end installed and commissioned in parallel with CMS operations before F.E.



Phase I HCAL frontend electronics upgrade

- HE frontend electronics → fabrication over, installation during early 2018 is ON.
- **HB frontend electronics→ fabrication & testing: 2017-2018, installation : 2019**

Responsibility of our group here for HE Front end electronics

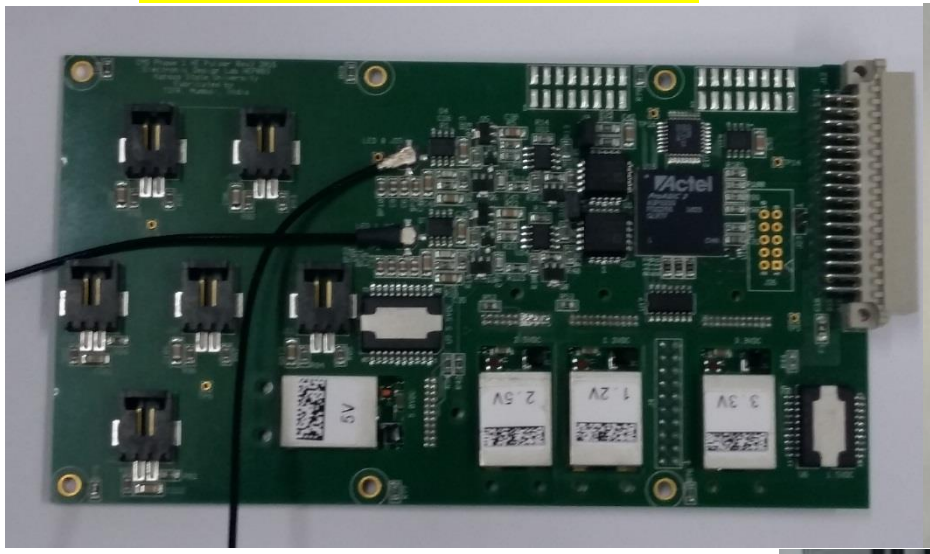
- 200 SiPM Control Boards (4 layers) each of 48channels + Bias Voltage cards
- 55 Calibration Units –along with the Aluminium Casings
- 60 Pulser Boards (6 layer PCBs) + peripheral boards

➢ Contribution in R&D stage → improvement of design based on
→ Experience of HE front end electronics helped in
→ Participation in July 2017 beam activities

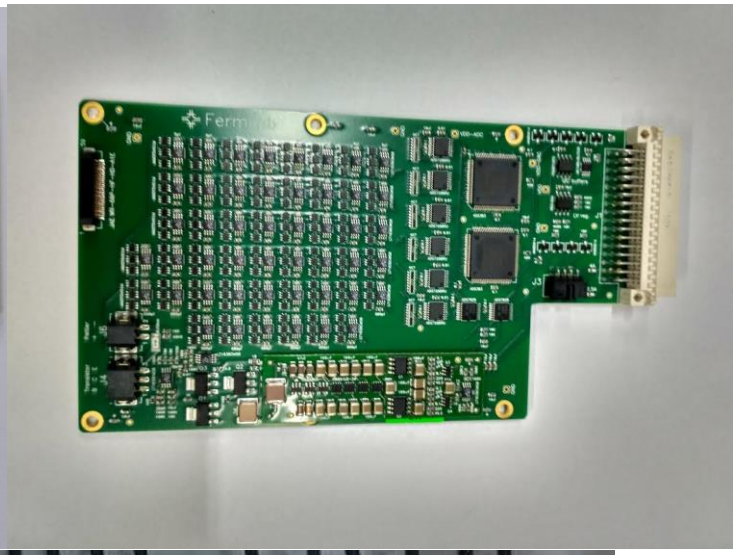
➢ Indigeneous quality assurance programme
➢ Full Fledged test stand at TIFR with MicroTCA and other Back End Modules

Boards for HE FEE made in India

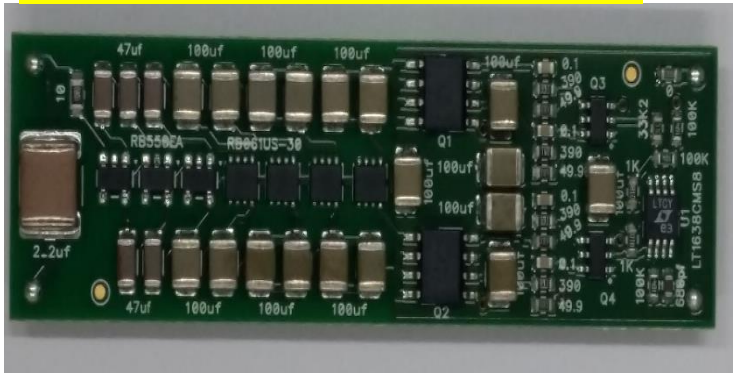
Pulser Board for CU



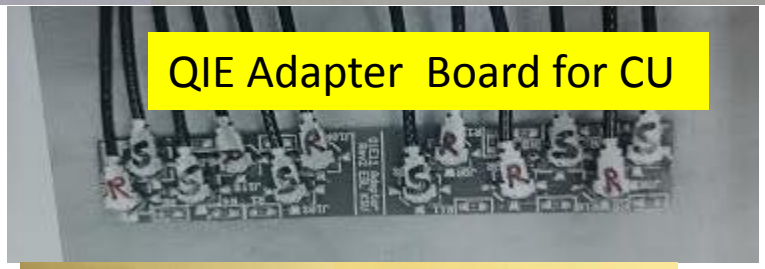
SiPM Control Board Board for RM

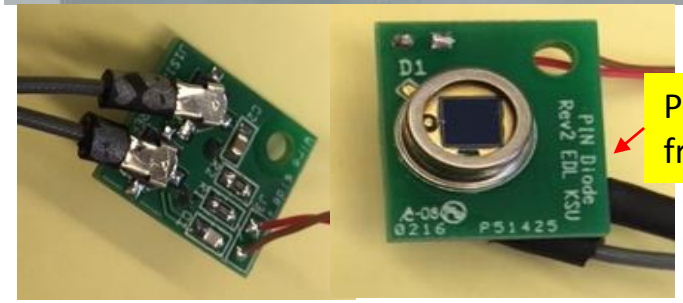


48 channel BV Board for RM



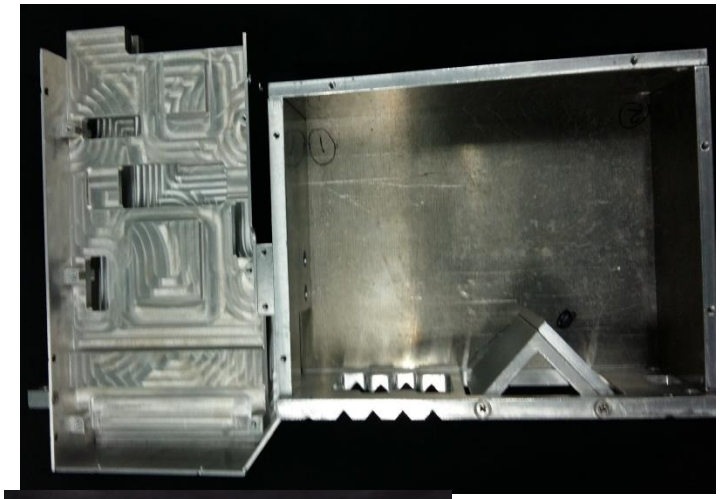
QIE Adapter Board for CU

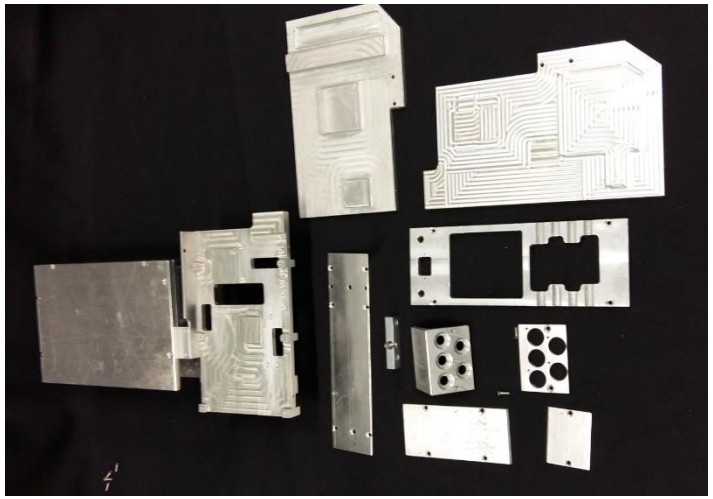


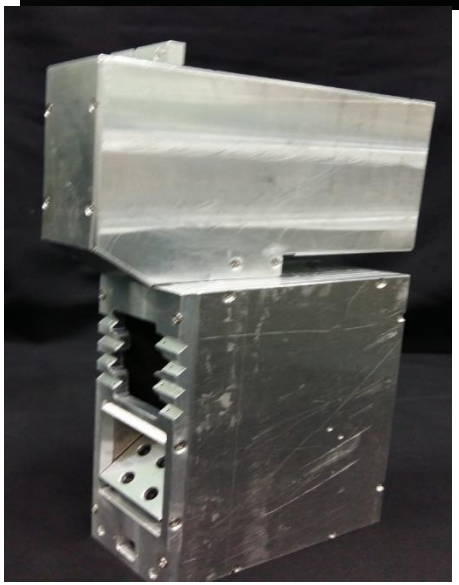


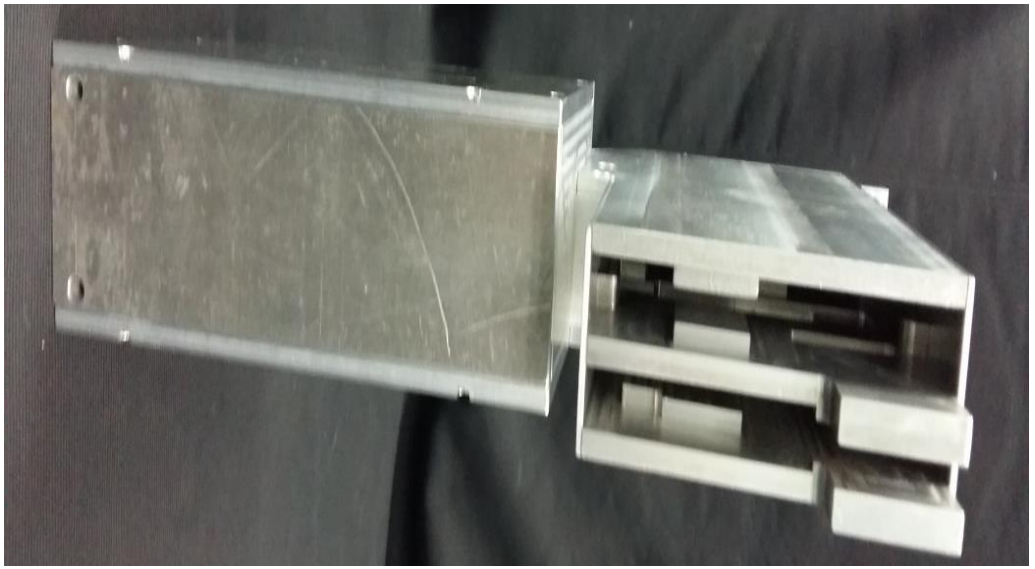
Pindiode board front side

HE Calibration Unit Mechanics









Test setup at TIFR for QC of FEE

The SiPM Control Board : Installed in the SiPM Readout Module (RM), provides the SiPMs with programmable individual bias voltage, measures SiPM Bias Voltage currents, drives Peltier element for SiPM cooling, measures the temperature and the humidity in the SiPM envelope and also does miscellaneous housekeeping things.

About 200 HE SiPM control boards were fabricated in India

- The application and the hardware to test these cards has been developed using the PyQt interface with the Raspberry pi-2 controller board .The application code developed in python uses the pigpio (pi general purpose input output) bus to do the I2C communication with the Clock and Control Board emulator (CCM).
- The ADC (Analog to Digital Converters) and the DAC (Digital to Analog) registers on the SiPM control Boards are successfully read out and controlled for data reading and writing.
- The user interface displays the results in parallel with the normal data taking task using the multi threading concept .

Test setup at TIFR for QC of FEE

The CU Pulser Board : Installed in the Ca;ibration unit, provides the LED light in a controlled manner to shien the same on the SiPMs and also on the Pindiode boards inside the Calibration unit

-About 50 such HE Pulser boards were fabricated and tested in TIFR

-Another 200 HE pindiode boards were fabricated and tested in TIFR

--About 60 Adapter boards were fabricated and tested in TIFR

--55 Calibration units made and assembled and tested in TIFR

- The in house developed test setup was again used to do the Quality control of the Pulser board that has a MicroSemi FPGA
- The Flashpro tool used to update the firmware of the FPGA
- Trained students to do this for some of the boards,thus introducing the circuit implementation in the FPGA. The firmware to produce pulses is developed in VHDL and Verilog HDL
- The Pulser board also has CERN DC DC converters which were separately tested too

Testing and calibrating SiPM control boards

- All SiPM control boards and Pulser boards were tested at TIFR in the past for HE with the Interface now be updated to test 64 Channels of SiPM Bias Voltage(HB) instead of 48 channels
- Instead of SiPM –resistance load on test board is used here.
- Tests for Bias Voltage actually going to all channels of SiPM:

 will be manually tested for 3 different Bias Voltages close to the operating BV

- Linearity test : measurement of current versus Bias Voltage .

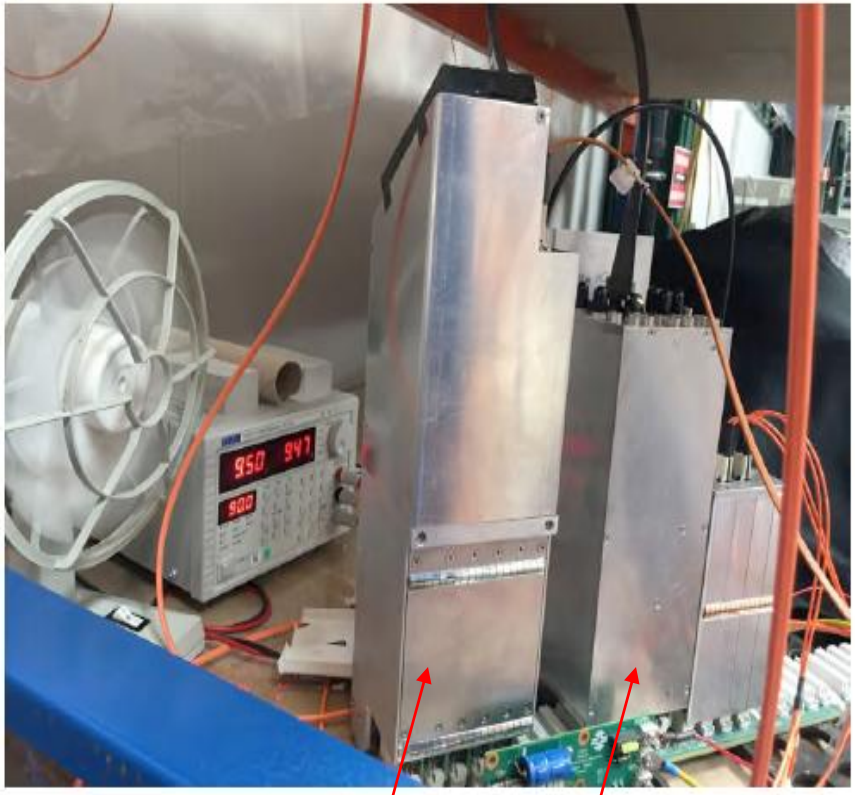
 will be recorded automatically for all channels of SiPM boards

- Using Standalone Raspberry pi setup with HE backplane.
- Students will work under my supervison

FEE Test setup at CERN

The first Prototype HB Readout Modules at cern being tested with HE backplane

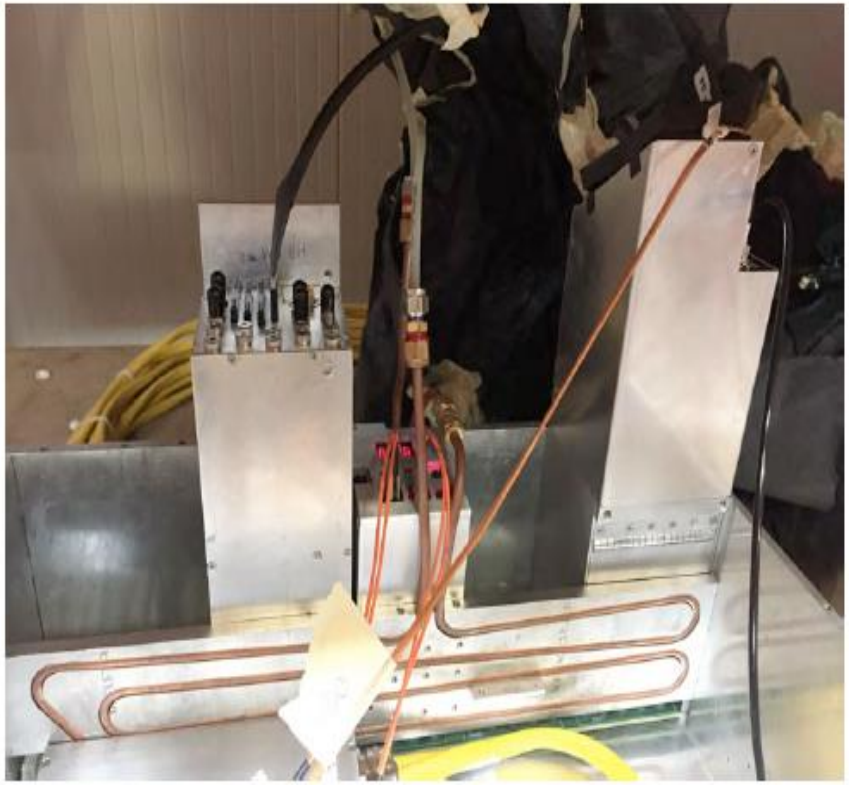
ngCCM, RM and CU in bare HE backplane



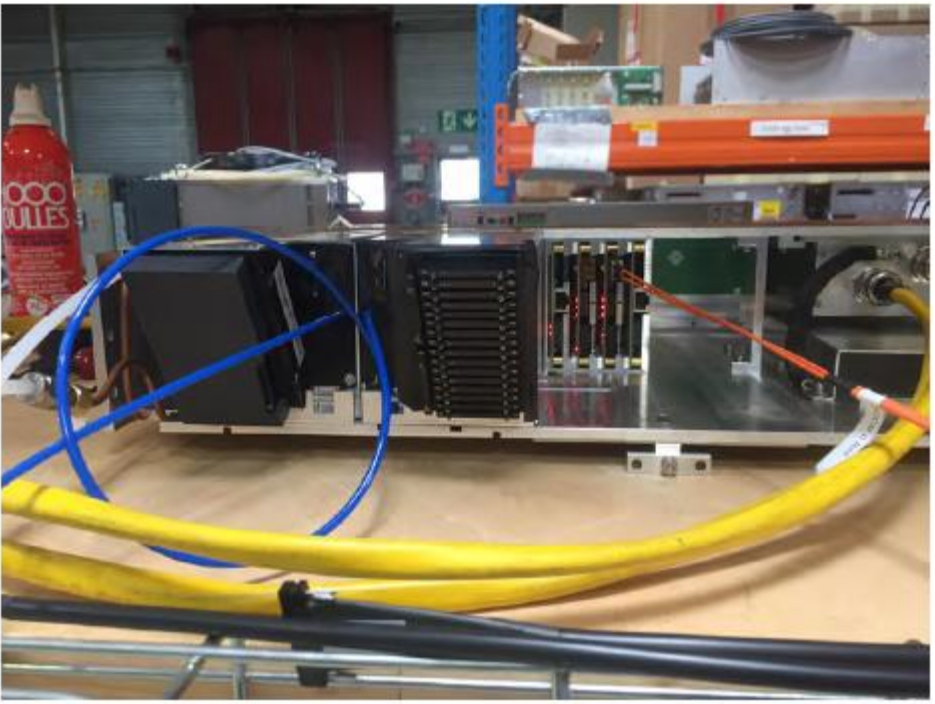
HB RM

HB CU

ngCCM, RM and CU in HE RBX



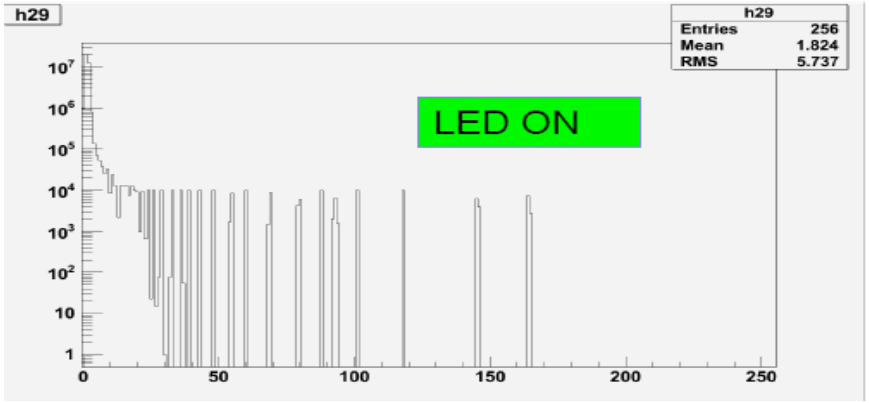
Full HB ngRBX during testing at CERN

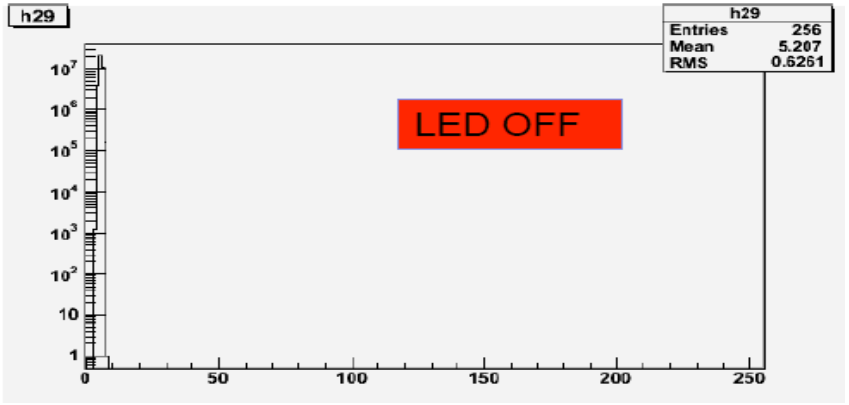


Test of the HB Prototypes in CERN

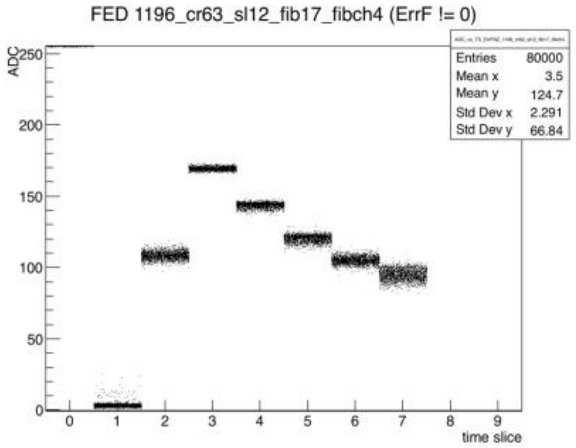
Test of the Calibration Unit

- We are able to send WTE with the AMC13 in loopback mode
- We verified that we can see light come from the HB Pulser board
- We have read the LED light through the pin-diode
- We also managed to time-in the LED (both for HE and HB using bxdelay scan). Data needs to be analyzed, though.
- The following ADC plots were made using HISTO/INTEGRATE mode of the uHTRTools

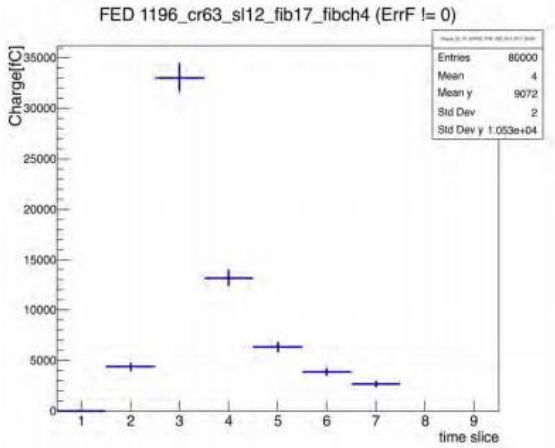


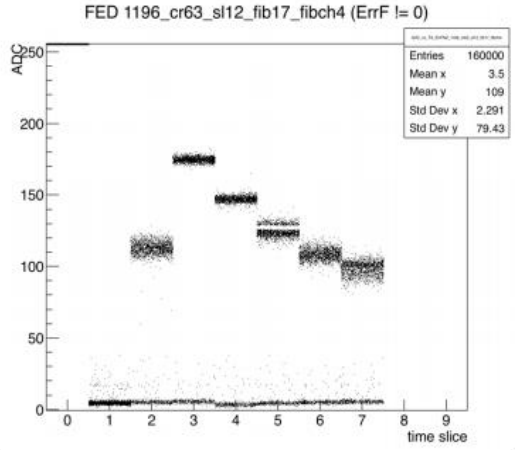


RM1,2 (LED light seen by SiPM

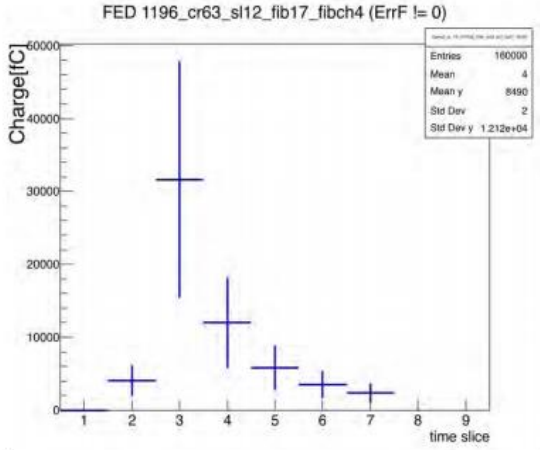


RM#1



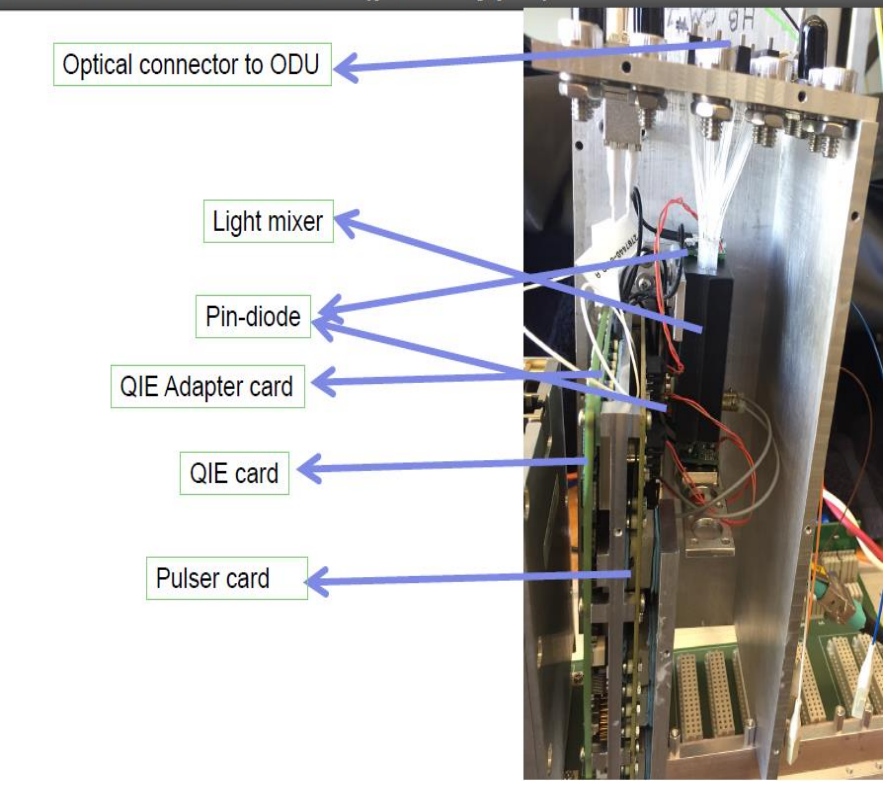


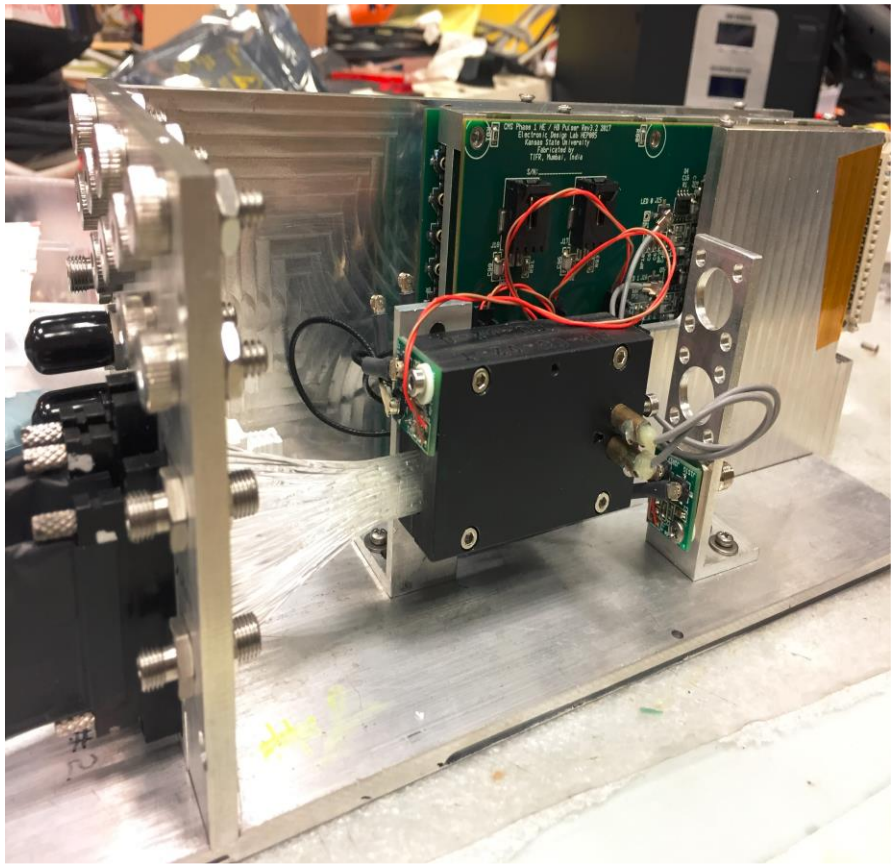
RM#2



HB Prototype Calibration Unit

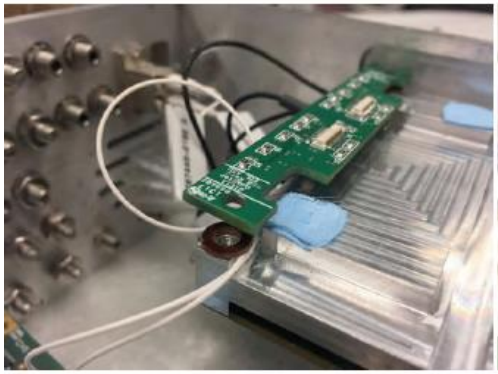
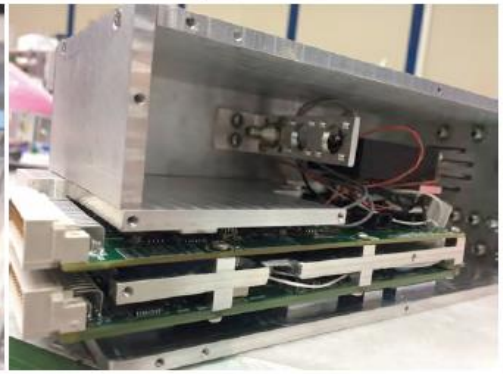
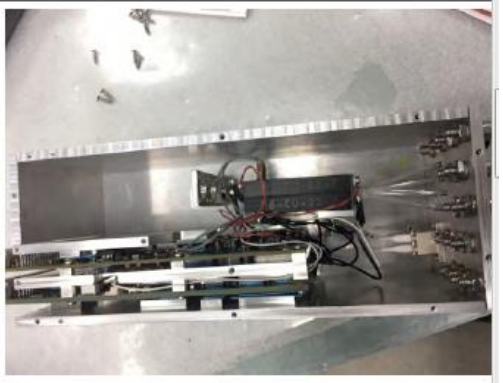
HB Calibration Unit (prototype)





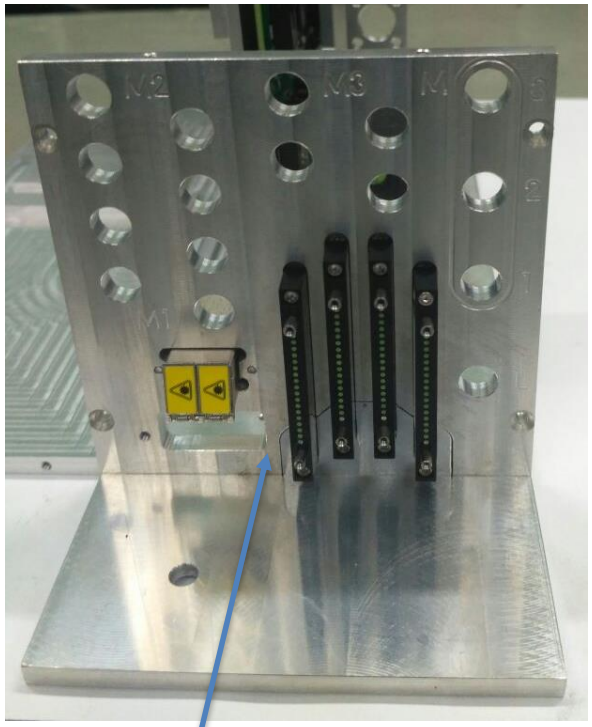
HB CU Mechanics changes

Issue with CU mechanics

- Need a washer at the connection of the adapter card and wall between 2 boards
- Need to cut the aluminum wall to avoid connection of the board and wall
- Need to chop a small piece on wall between 2 boards to avoid QIE Jtag hitting the wall

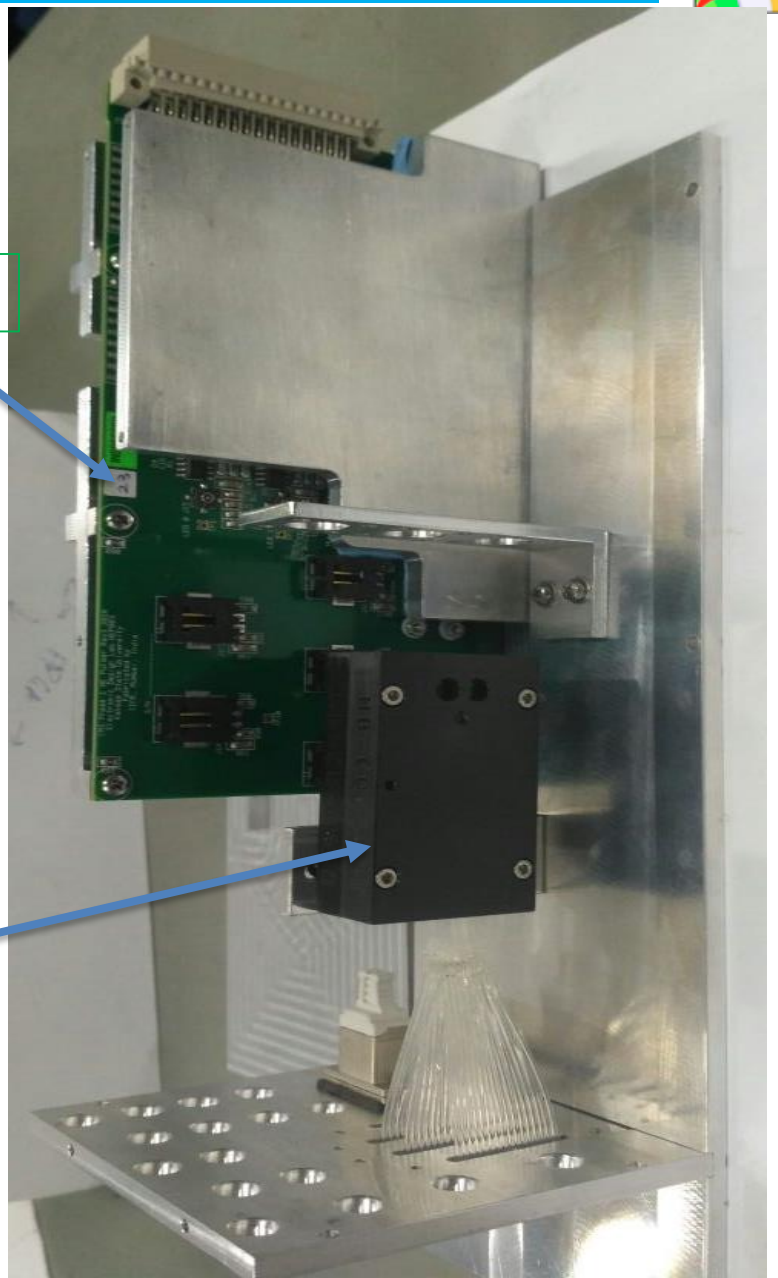
Second Prototype made in TIFR Workshop



Front Plate of CU with connectors

Pulser Board

Black optics box with light mixer



HB FEE Cards and HB Calibration Units

Pulser Board for CU

- Used to control the LED light that is made to shine on the SiPMs during Led calibration test

SiPM ControlBoards: 200 total (1 SiPM Board/RM and one BV Board/RM

====

150 for the detector

30 spare

10 Burn In test stand

5 irradiation

5 accelerated aging

CU: casings 55 & 60 cards total

====

36 for HB detector

8 spares

10 for test stand

1 CU for irradiation

1pulser Board/CU

5 pulser cards for accelerated aging

Status of HB FEE cards Production

- Have initiated the process of getting 5 prototype SiPM control boards made with order placed and procurement of components started

→ 10 prototype boards will be delivered by May mid week and testing follows after that in TIFR and retesting at CERN

- Just got the final design of the mezzanine Board.
- Time reqd. to test prototype cards at Mumbai and CERN: 2 weeks orso

➔ go ahead for card production: ~ 6 weeks from design finalization.

- Pulser cards HB CU: →10 cards work in progress and to be delivered by may middle (non commercial components bought and provided to the fab)

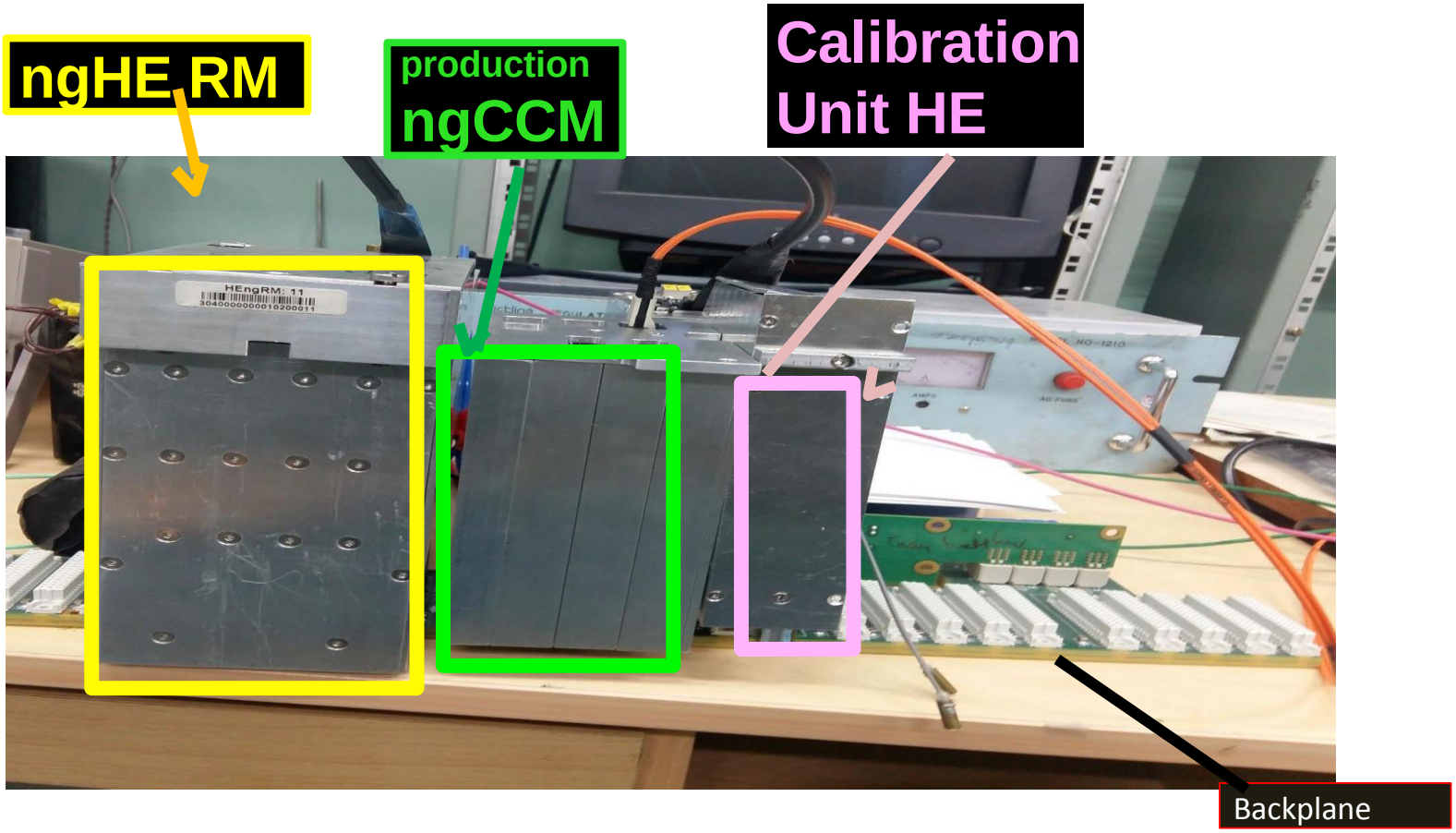
(i) pin-diode PCBs → total # needed 180+spares =200 PCBs ready

→ Assembly will be done in-house by our technician with pin-diodes and other components procured

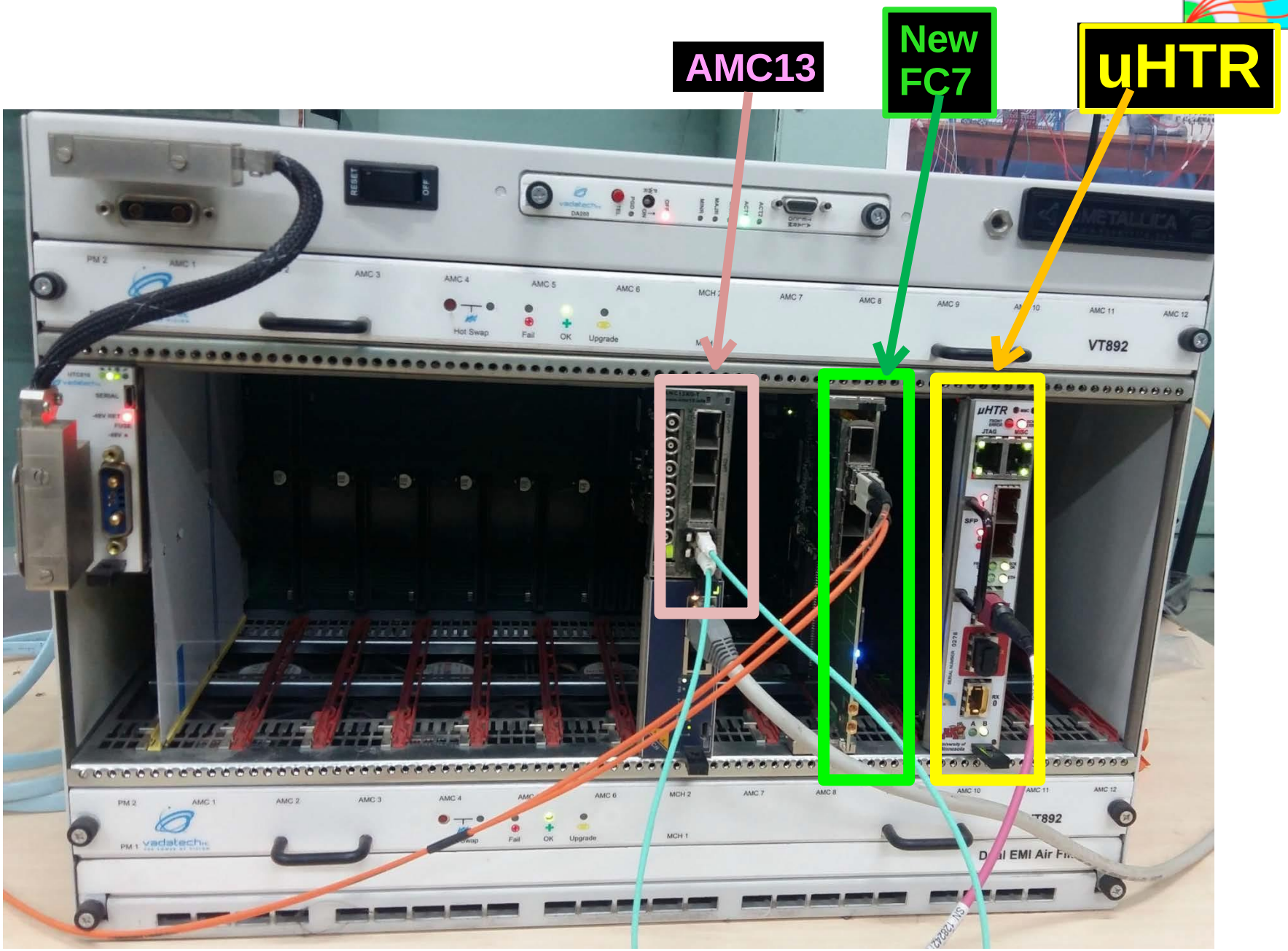
(ii) QIE adapter boards (total #: 60) to be delivered by May 2nd week

(iii) Jtag board PCBs : Order for fabrication to be initiated soon

Front-end setup at TIFR



Back-end Setup at TIFR



Plans for testing HB FEE cards

- Calibrate the SiPM Control Boards for their Bias Voltage on each channel with a resistor load connected instead of actual HB SiPMs and QIE not being currently available at TIFR
- Retest the SiPM Control Boards at CERN using HB SiPM in HB RMs

- HB CU to be mounted with the Pulser boards and QIE Boards (if available)on the backplane and tested for LED controlled light shining (using HE backplane for the time being, HB backplane when available)
- If we get a HB RM, we can test the SiPM control cards also in TIFR setup that is almost like the FNAL-type test stand (HB FE integrated with the BE) at TIFR:
  - Front HE RM,HB CU on the HE backplane with external power supply of 9V
  - ngCCM, uHTR , ngFEC, AMC13 are at the Backend in the MicroTCA crate
  - Taking LED and Pedestal runs with the RCMS setup also at TIFR-DAQ

Gist of the data acquisition method

- New on-detector QIE electronics cards will transmit data at 4.8 GHz to the new µHTR cards residing in µTCA crates in the CMS electronics cavern.
- The µTCA crates are controlled by the AMC13, which accepts system clock and trigger throttling control(TTC) from the CMS global DAQ system.
- The AMC13 distributes the clock to the µHTR and reads out data buffers from the µHTR into the CMS data acquisition system.
- The AMC 13 also provides the clock for in-crate GLIBs which in turn distribute the clock to the on-detector front end electronics.

Status of integrated test-stand at TIFR

- The communication between HE RM, ngCCM & Backend done successfully.
  - Tested the HE Pulser board LED in ON & OFF states with the register commands operating the ngCCM server
  - Can read LHC clock and also the firmware on the AMC13 and FC7 FPGAs
  - Using uHTRtool can dee the dump of raw data
- HCAL online software (HCOS),RCMS, Tomcat, MySql, MySQL WorkBench being installed and other pre-requisites
  - Database templates received are being updated according to TIFR Setup with the help of DuckCAD tool (Thanks to Puneet from TIFR)
  - RCMS web navigation configuration troubled us initially but finally launched it.
  - We are still under process to setup confmagik with editing configuration table contents locally and updating them using DuckCAD
  - Setup snippets /CfgCVS will be the next step
- Once RCMS fully tested, subsequent tests are:
  (i)timing scripts, (ii) LED & pedestal runs
- Better cooling arrangements to be implemented soon.

Purpose of the test stand at TIFR

- Prototype hardware testing under time constraints and get started with understanding of the MicroTCA standard

- On-site technicians often do low-level hardware tests and hardware modifications (sometimes on electronics for important data taking)

- This often goes along with testing Hardware/FW development support which can be done here and integration of any new hardware

- Test stand will be used for the quality control testing of the ngHB FEE Cards both the SiPM control cards calibration and CU Pulser boards QC

- Train students for the DAQ hardware and firmware details

Summary

- Successfully delivered the HE FEE boards and HE Calibraion Units
- Enriching experience to learn about new things like FPGA ,use of Various repositories and software tools
- Setting up the RCMS integrated stand with MicroTCA backend has been challenging and also a backbone to use and develop MicroTCA based modules in future
- Looking forward to the commitment of development of HB FEE and Quality control of the same in TIFR
- Thanks for the cooperation of all DHEP members