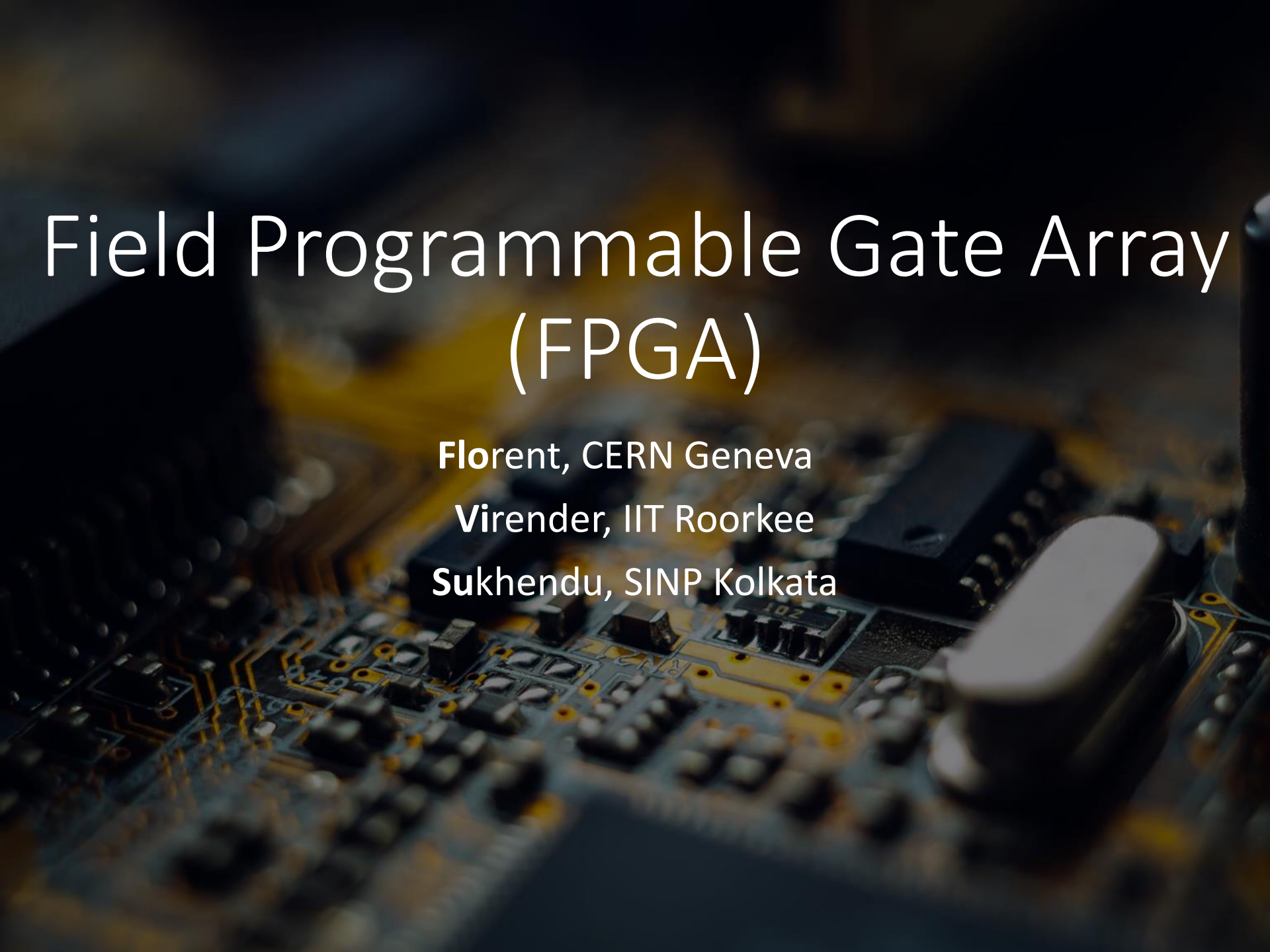


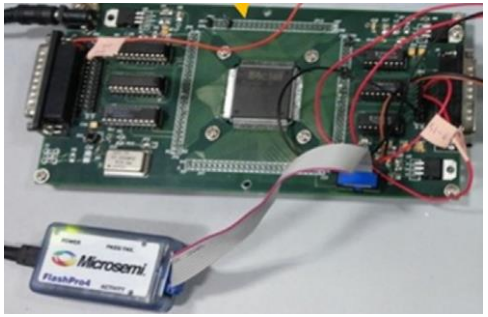
# Field Programmable Gate Array (FPGA)

**Flo**rent, CERN Geneva

**Vi**render, IIT Roorkee

**Su**khendu, SINP Kolkata

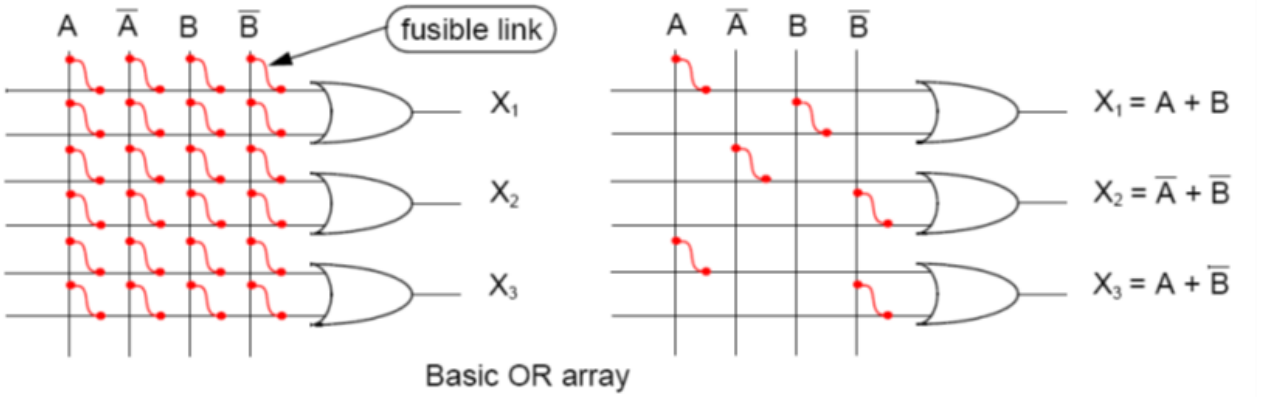
# Different kind of electronic boards





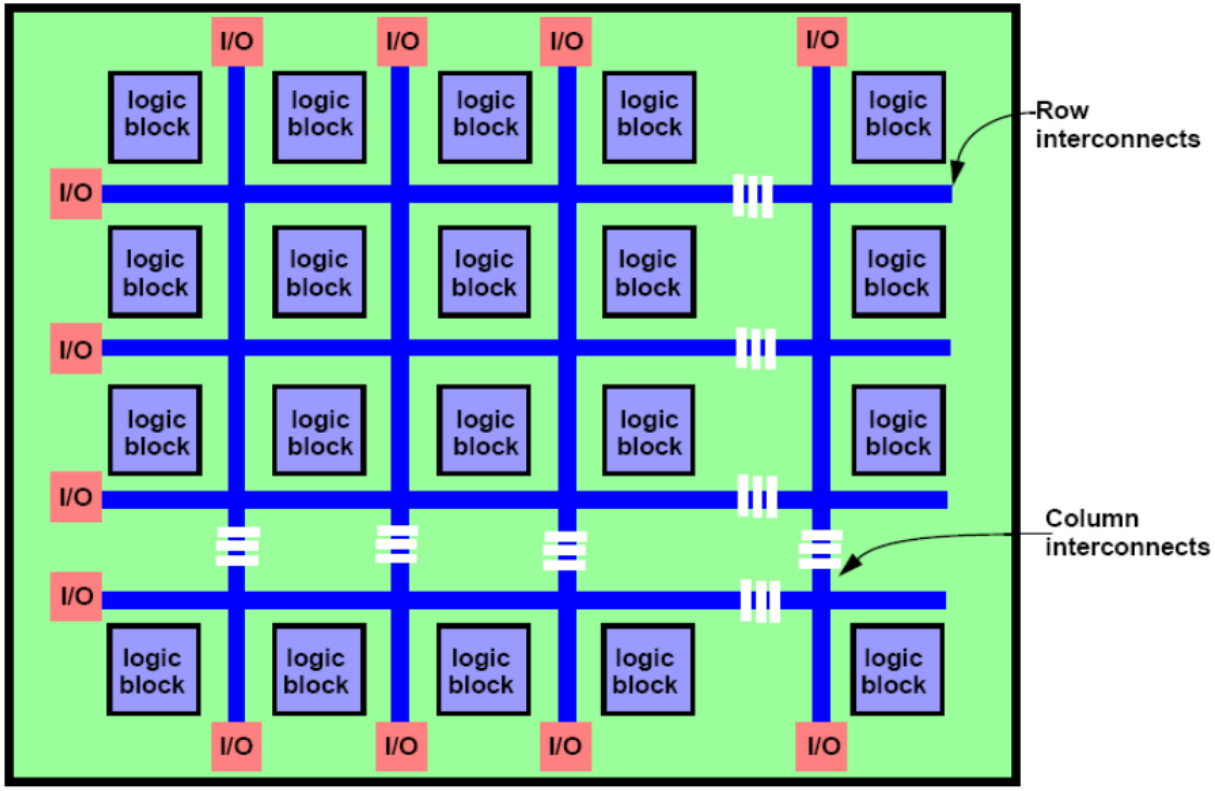

| CPU | FPGA | ASIC |
| --- | --- | --- |
| Very Versatile | versatile | Not versatile |
| electronic circuitry that executes instructions such a computer program | matrix of configurable logic blocks that are connected by programmable interconnects. | silicon chip designed for a specific logic |
| Consumes more power | Power efficient | Very power efficient |
| Very slow | fast | Very fast |
| Intel i3, i5, i7<br>Apple silicon M1,<br>AMD Ryzen processors | smart power grids<br>real-time detection of objects,<br>Identification of faces<br>robots | LCD display drivers<br>Thermal controller<br>Biometric sensors<br>Engine monitoring sensors |

The first programmable chips were Programmable logic arrays(PLA). It consisted of structures of AND and OR gates with user programmable connections. Today such devices are generically called Programmable Logic devices(PLDs).



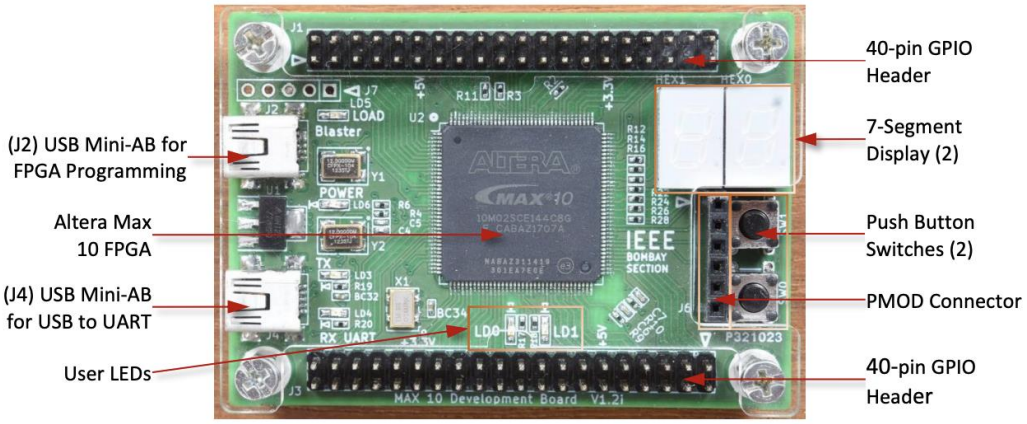
- A complex PLD (CPLD) is nothing else than a collection of multiple PLDs and an interconnection structure.

- Compared to a CPLD, a Field Programmable Gate Array (FPGA) contains a much larger number of smaller individual blocks + large interconnection structure that dominates the entire chip.

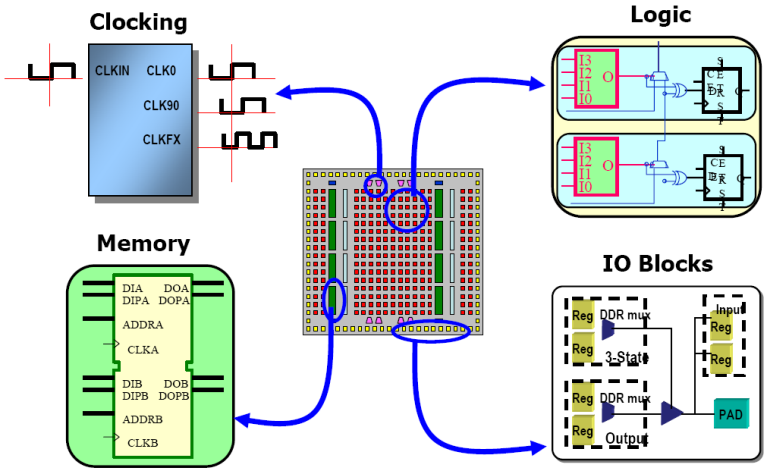


# Basic FPGA architecture

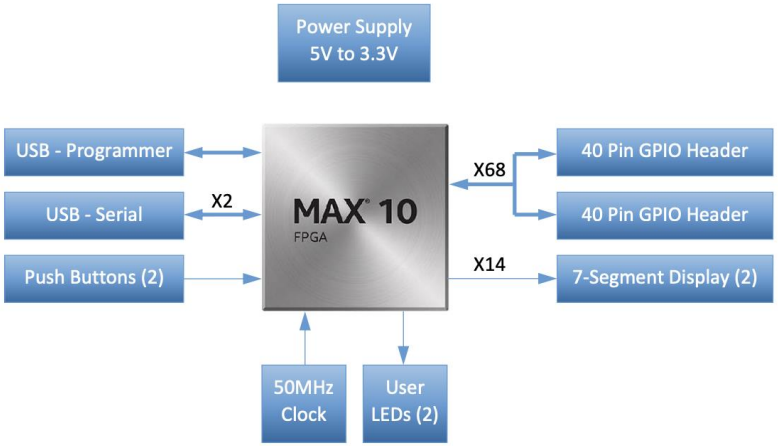
Max10 devKit




FPGA

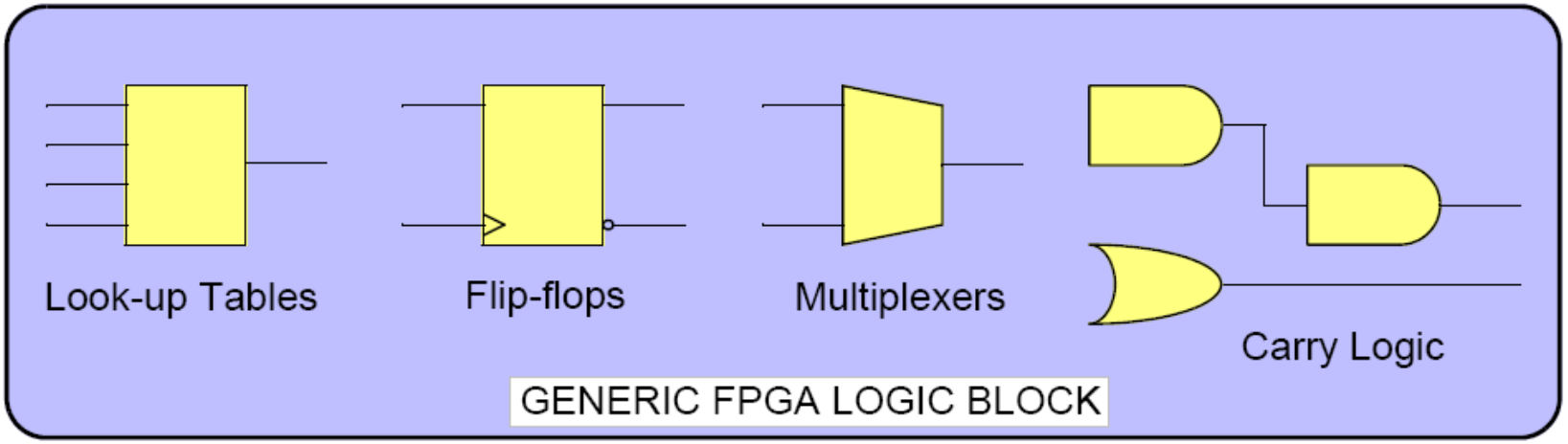



Block diagram




- Mainly used in real-time systems where response time is crucial, where the hardware configuration is likely to be changed
- An FPGA can execute several operations in parallel

# Logic block



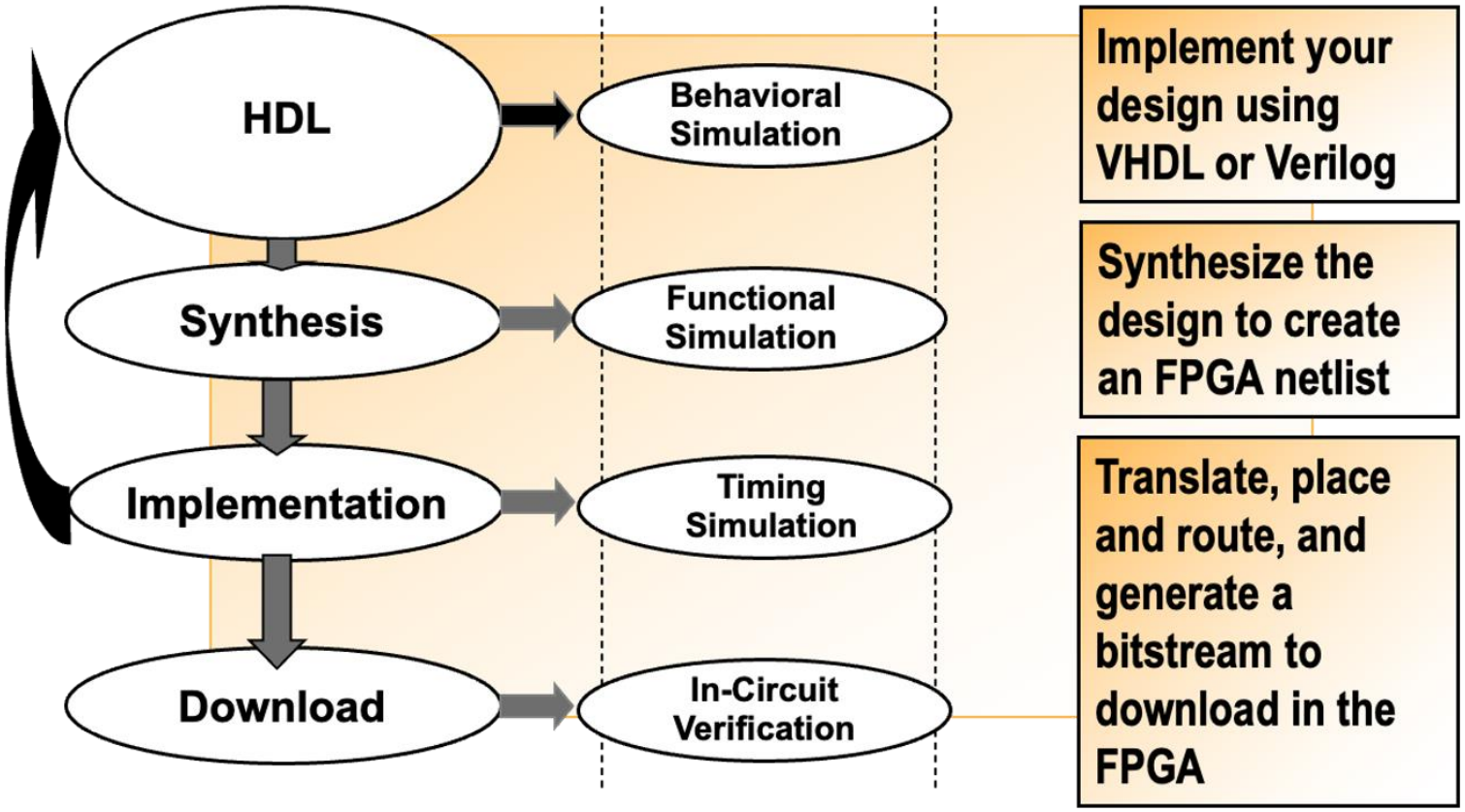

Configurable logic blocks are the heart of an FPGA
Always contains:

- One or more look-up tables (LUTs) with three or four inputs
- D Flip-Flop (a digital electronic circuit used to delay the change of state of its output signal)
- Output.

These blocks create a physical network of logic gates that can be customized to perform specific computing tasks.

Many other elements can be added,
CPUs, memory controllers, USB controllers or network cards, ...

# Design flow




- Hardware description language such as VHDL or Verilog, computer languages that allow to describe an electronic circuit and its behavior
- An HDL simulator to design a circuit and verify its operation.
- A binary file is generated using the FPGA manufacturer's proprietary software
- Then implemented in the FPGA

# Programming a FPGA

- FPGA developer: write code that describe physical structure to be built
- Other programmer: write code that control how the structure operate or it use
- Example: in the case of adding 2 numbers FPGA developer will write code that will describe the digital circuit that add the 2 numbers together

```
library IEEE;
use IEEE.std_logic_1164.all;
entity andd_Gaate is
    port(A: in std_logic;
         B: in std_logic;
         Y: out std_logic);
end andd_Gaate;
architecture andLogic of andd_Gaate is
begin
    Y <= A AND B;
end andLogic;
```

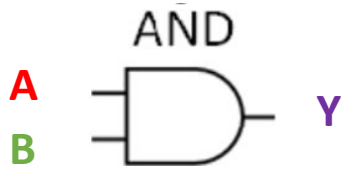
Code divided in 3 part

- Library
- Entity => declaration of all input/output we will need
- Architecture => map the entity to make the function needed

# Simulation

- Compiling FPGA code can be very long
- Before compiling simulation can be a good idea !!!

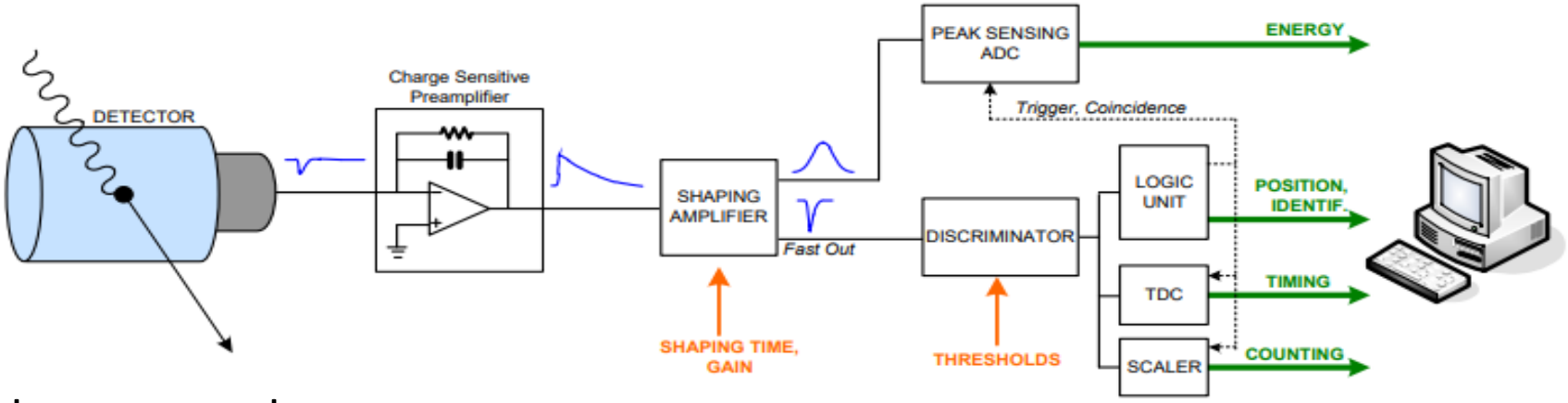
- Example of simulation for an AND gate
  - Input A, B
  - Output Y




| INPUT | | OUTPUT |
|---|---|---|
| A | B | |
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

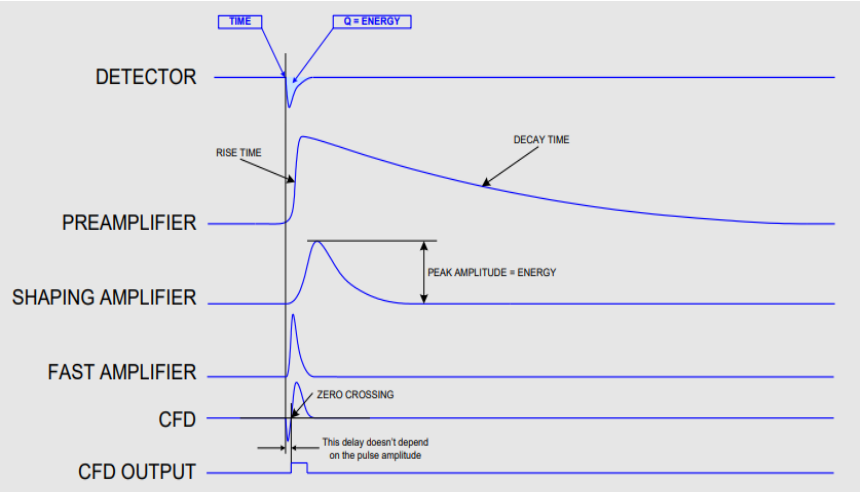
# Where we have used the FPGA

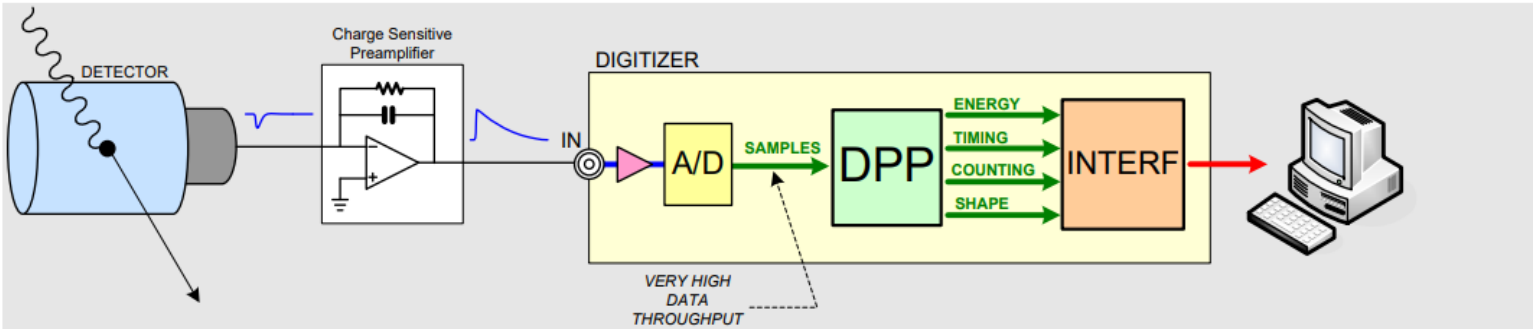
- Technicalities we have learn in FPGA lab
- IO scintillator --- Digitizer and in Cherenkov detector setup



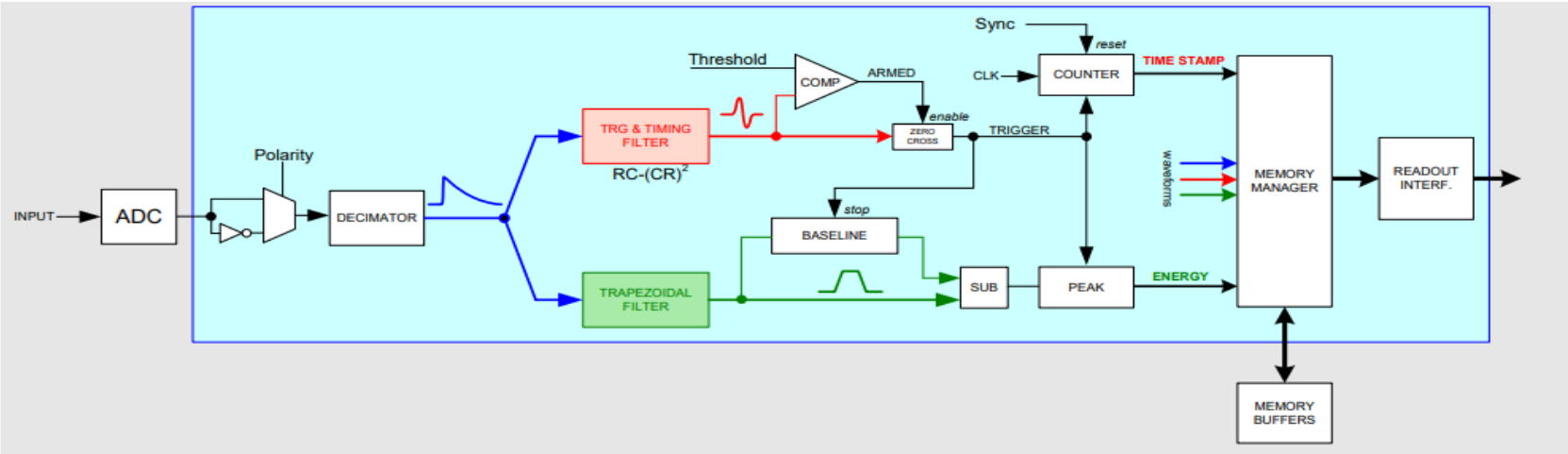

## Analog approach

- The block diagram shown the steps of signal readout from a detector.
- In each steps the necessary module is necessary according to the requirement for the detecting particles.






- In the digital approach all blocks from the shaping amplifier to the PC are synthetized into a single device, the digitizer.
- FPGA based techniques allow the user to change the readout parameters according to the detector characteristics, thus enabling the measurement of different radiations with different detectors using the same hardware. The digitizer becomes itself a Digital Multi Channel Analyzer (MCA).
- For the specific application FPGA firmware to be loaded.
- A 14-bit ADC resolution allows a 16 K “Channels” Spectrum to be generated. The spectrum resolution should be matched with the detector Energy resolution.

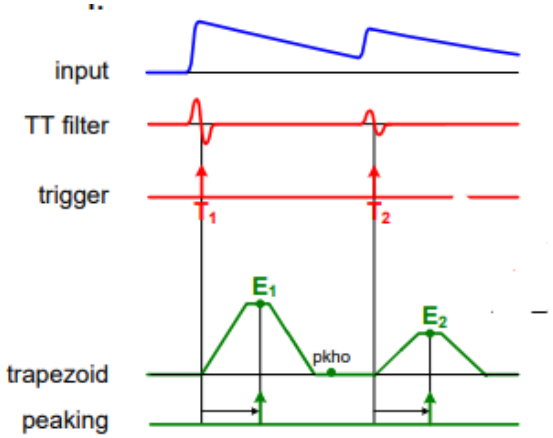


## Decimator

- When the signal is particularly slow, hence it is necessary to set values for the DPP time parameters that are not within the allowed range. The effect of the decimator is to scale down the sampling frequency of a factor 2, 4 or 8. The decimation applies to the energy filter only.

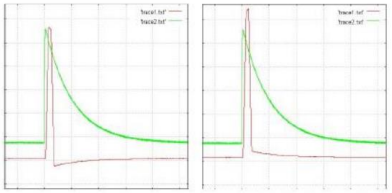
## Trigger and Timing Filter (TTF)

- Generate a digital signal that identifies the pulse and calculate the time occurrence of event.
- Digital RC-CR2 filter—zero crossing make a trigger stamp.
- Trigger logic get armed at the threshold crossing.



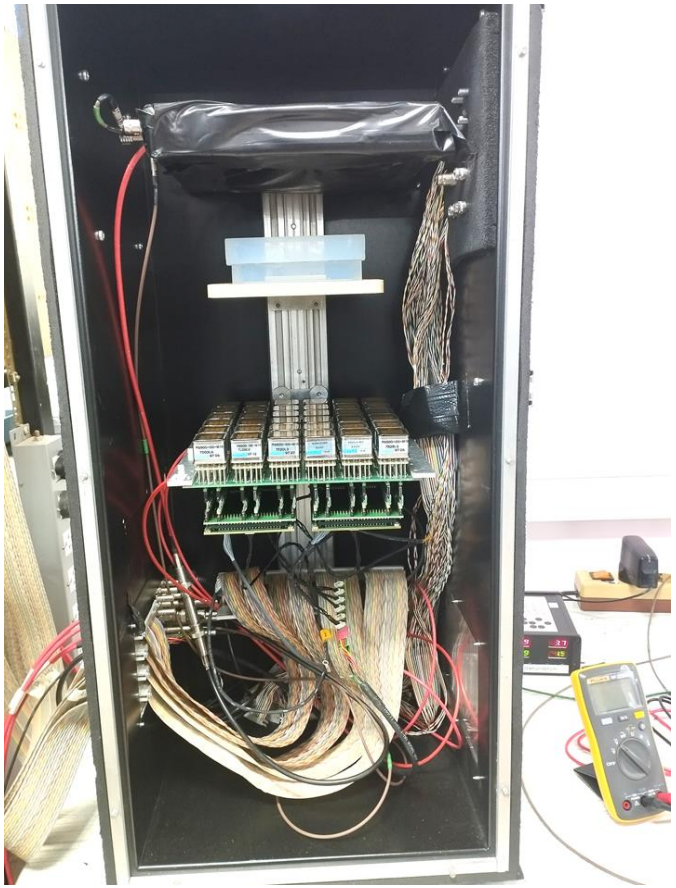

## Trapezoidal filter

- The shaping amplifier is able to convert the exponential shape from the Charge Sensitive Preamplifier into a Gaussian shape whose height is proportional to the pulse energy, in the same way the Trapezoidal filter is able to transform it into a trapezoidal signal whose amplitude is proportional to the input pulse height (energy).
- Peaking is in the flat region of trapezoid.
- Like the Gaussian pulse of the Shaping Amplifier, also the trapezoid requires an accurate pole-zero adjustment.



# Cherenkov photon detection

- Left one is readout of a single PMT with analog approach.
- Right one is the readout of 16 PMTs with FPGA board.



Thank You...