R&D activities on HGCAL electronics

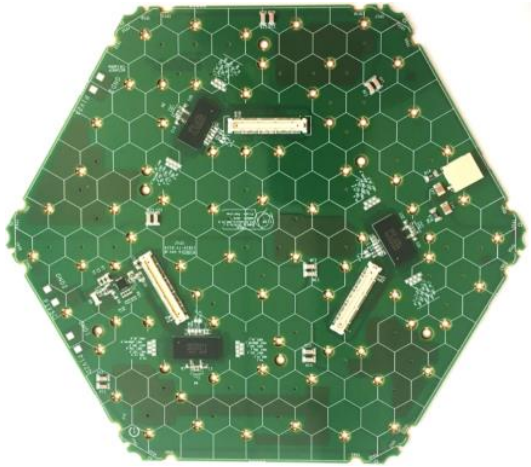
DHEP - TIFR, 05/05/2022

HGCAL - Overview

CMS HGCAL: 52-layer sampling calorimeter for phase-2 upgrade with unprecedented number of readout channels

Active Elements:

- Hexagonal modules based on Si sensors in CE-E and high-radiation regions of CE-H
- Scintillating tiles with SiPM readout in low-radiation regions of CE-H



8" Si Module

Electromagnetic calorimeter (**CE-E**): **Si**, Cu/CuW/Pb absorbers, 28 layers, 26 X_0 & ~1.7

Hadronic calorimeter (**CE-H**): **Si** & **scintillator**, steel absorbers, 24 layers, ~9.0

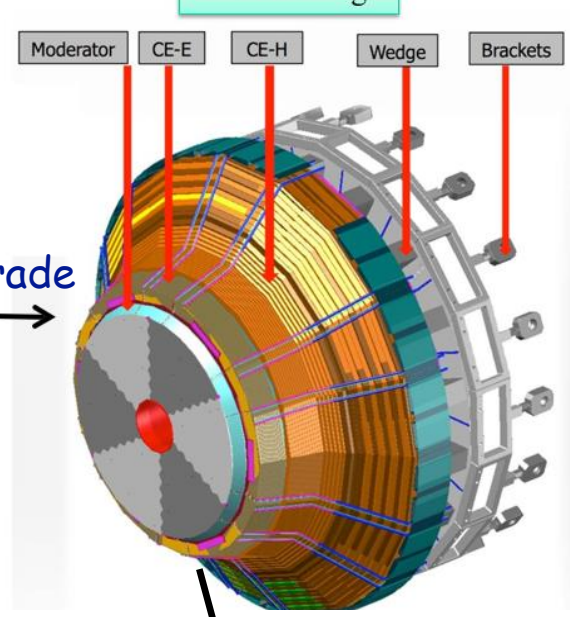
Key Parameters:

- HGCAL covers $1.5 < \eta < 3.0$
- **Full system maintained at -30°C**
- **~600m²** of silicon sensors
- **~500m²** of scintillators
- 6M Si channels, 0.5 or 1.1 cm^2 cell size
  - Data readout from all layers
  - Trigger readout from alternate layers in CE-E and all layers in CE-H
- ~27000 Si modules

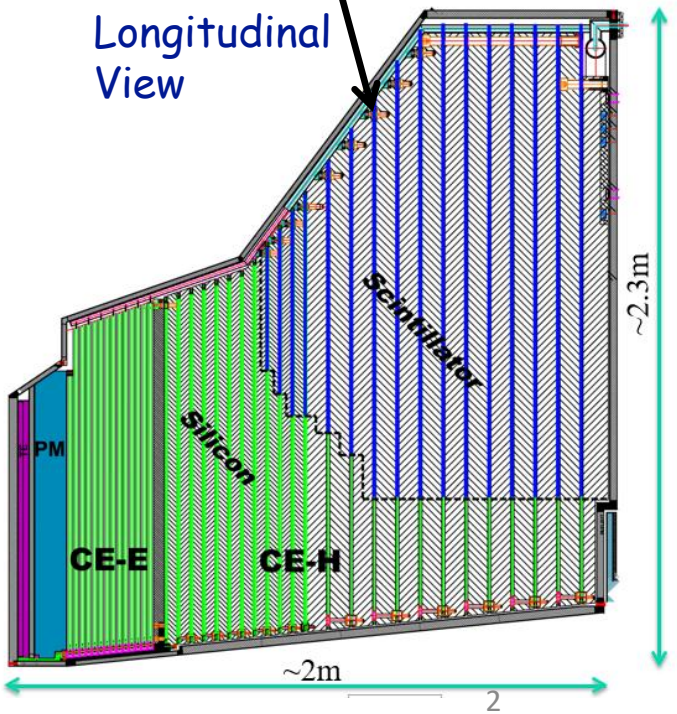
Present CMS endcap calorimeters

Upgrade

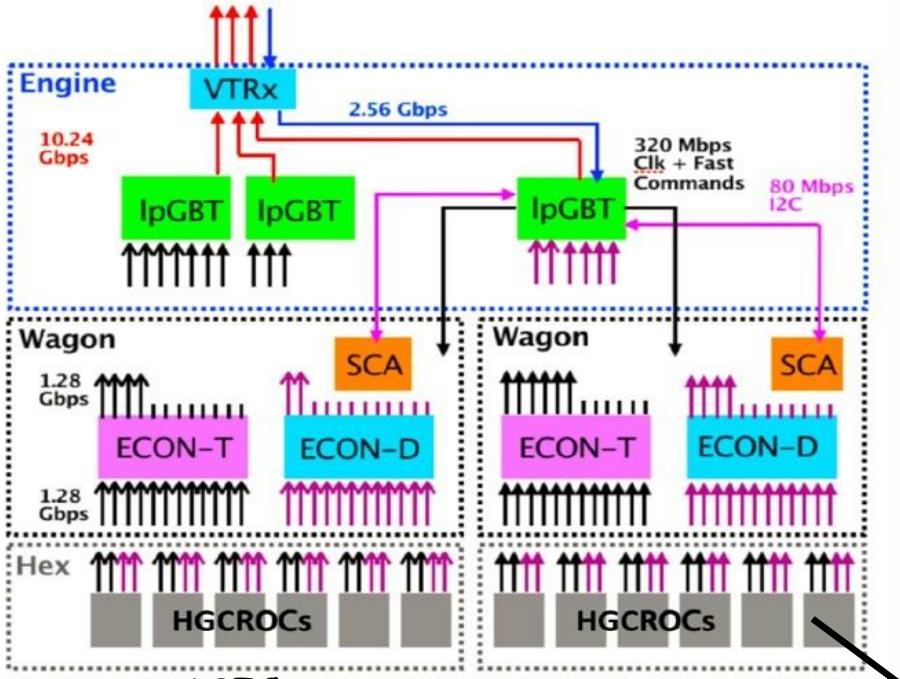
HGCAL design

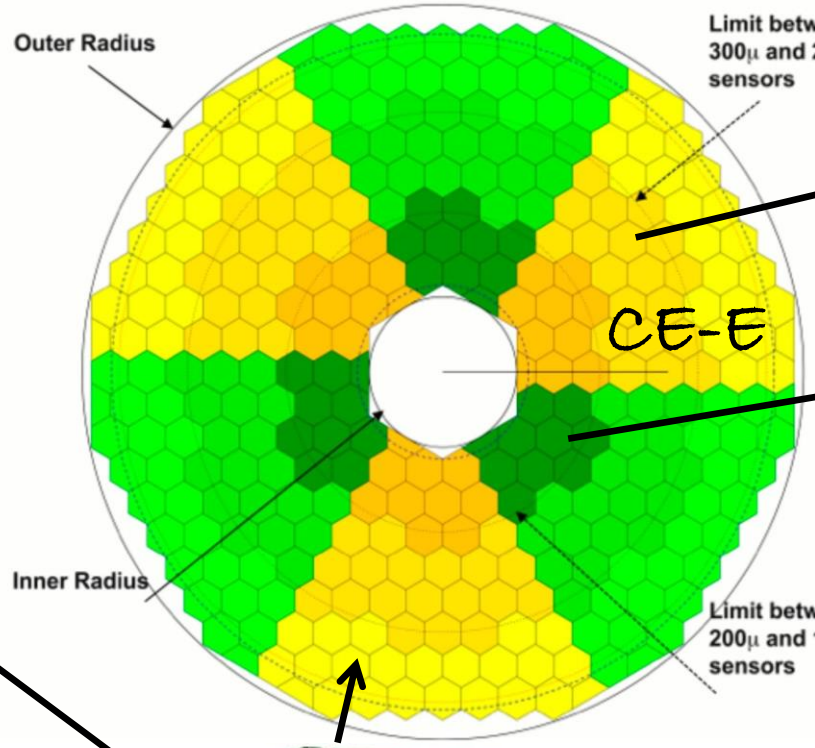


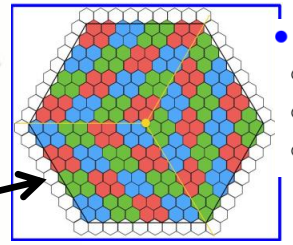
Longitudinal View



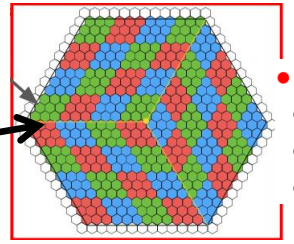
HGCAL Frontend Electronics - On Detector (Silicon Module Section):







- **Low density modules (LDM)**
  - 192 channels
  - cell size = 1.18 cm²
  - Outer radii



- **High Density Modules (HDM)**
  - 432 channels
  - Cell size = 0.54 cm²
  - Inner radii

Si-Module:

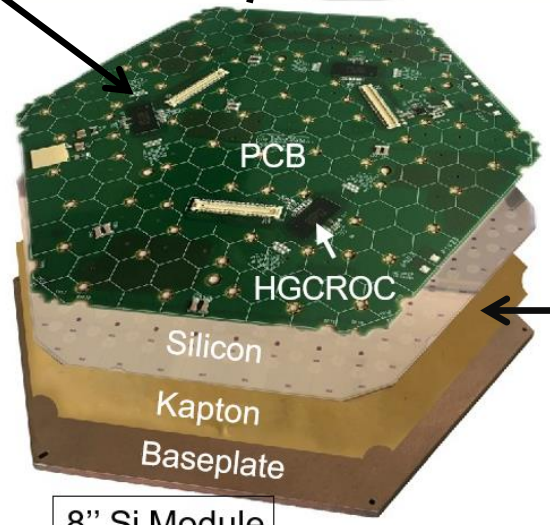
Glued assemblies, made with standardized Gantry, wire-bonders, encapsulation

Sends bunch crossing synchronous data to concentrators

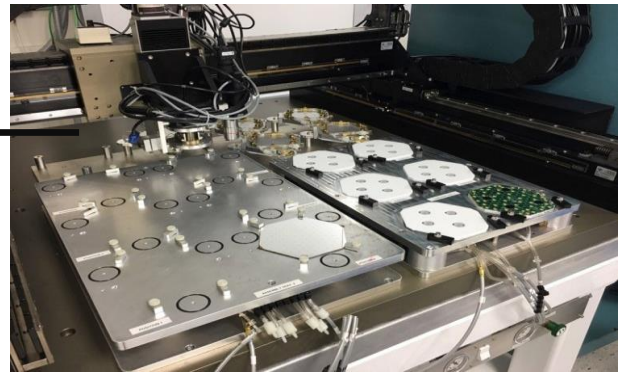
Concentrator ASICs:

ECON-T (trigger): selects trigger data before transmitting to the BE

ECON-D (DAQ): sends zero suppressed fine granularity data to the DAQ



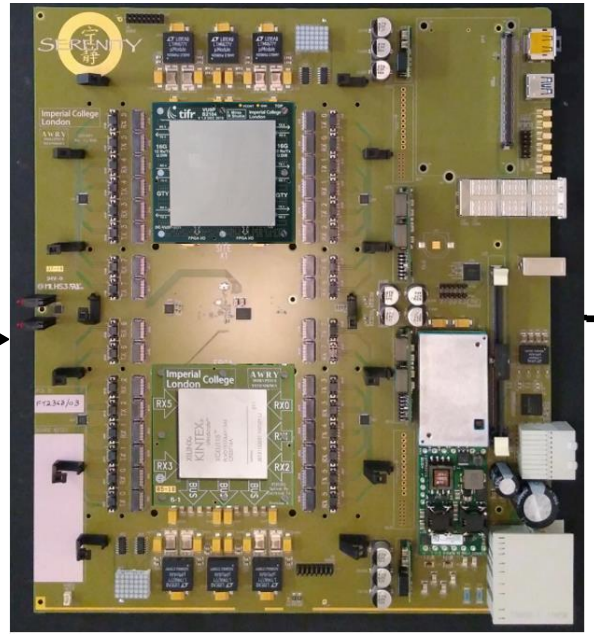
8" Si Module

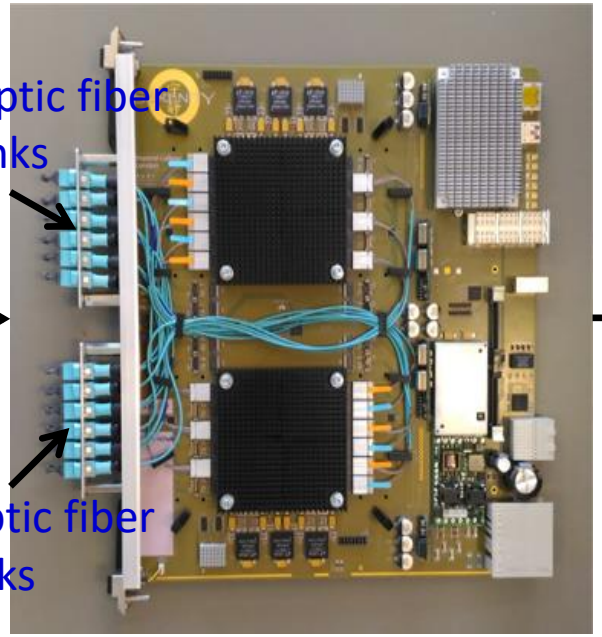


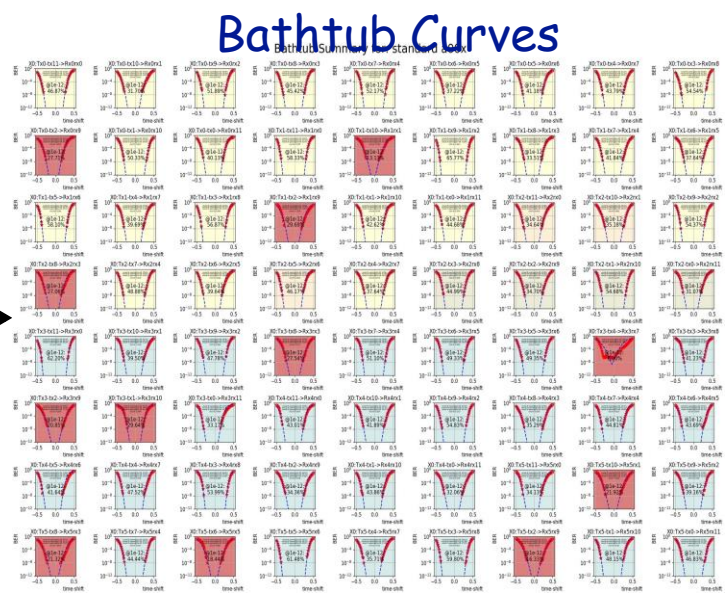
Plans (Fabrication + Assembly):

- Si Moules (Frontend)
- Baseplates with Kapton (PCB + Cu/W) (Frontend)
- Daughtercards (Backend)
- ATCA (Serenity) (Backend)

Off Detector Hardware: Flexible ATCA "Serenity" baseboard + Daughtercards (DCs):

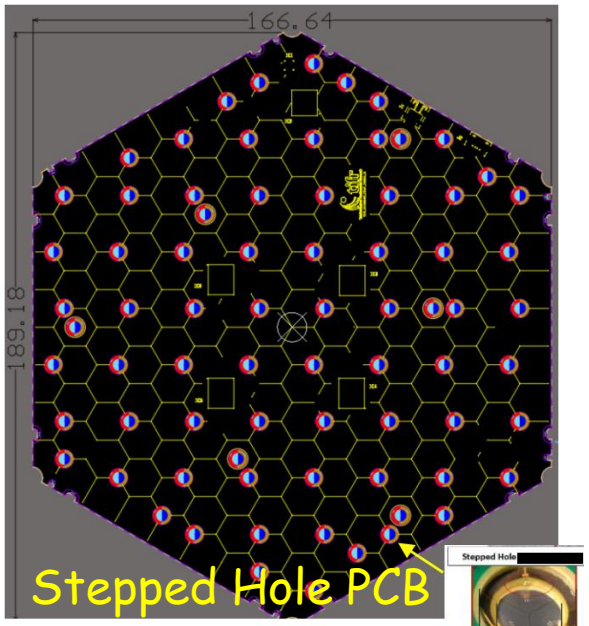


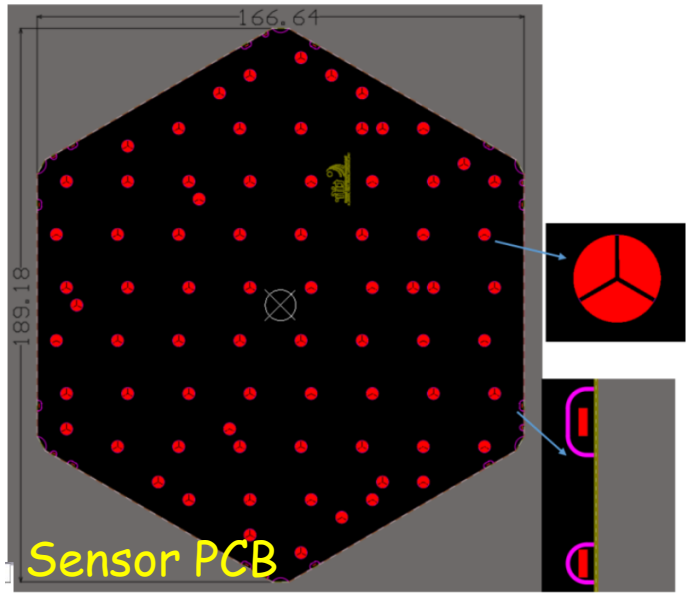


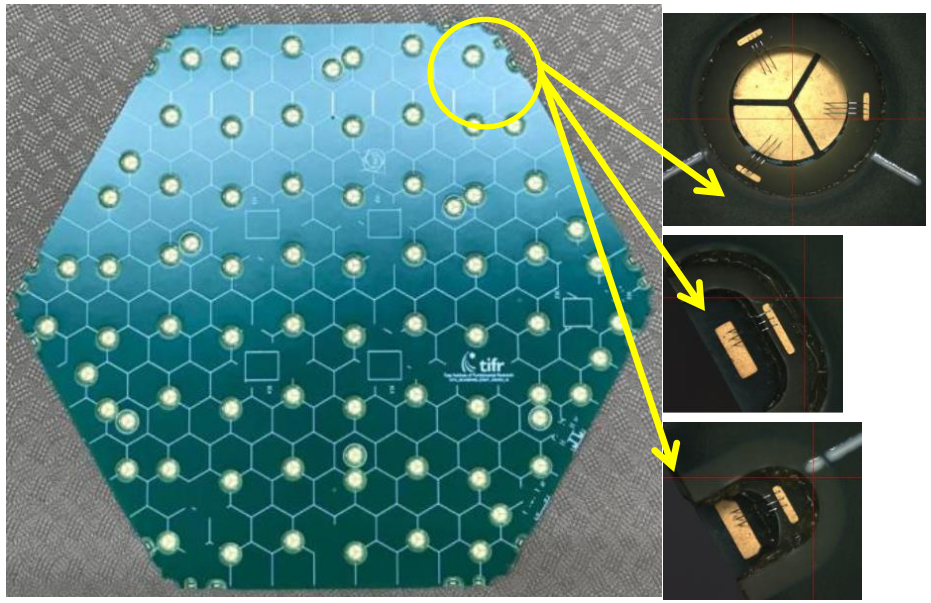


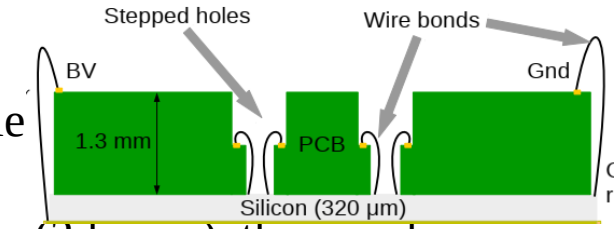
- Can host different types of powerful FPGA (Mounted on Interposer - ~2k pins)
- Generic motherboard common to other subsystems (versatile). DAQ & TPG will use different FPGAs for each baseboard (cost efficient) Up to 72 in and 72 out links (link speed up to 25 Gbps)
- Xilinx VU9P (SO1 & SM1) DCs, 16 layers complete in house design layout – 64mm x 64mm(Class 3 – HDI(High Density Interconnect)) – V1 done by SiPM group - DHEP, Fabrication and Assembly indigenously in India, Testing at CERN
- One of the MGT links swapped. 12 MGT(Multi Gigabit Transceiver) links with less than 30% performance
- PCIe enumeration at GEn1 instead of Gen2 on Atom ComE, Gen3 on i5 ComE
- DC layout upgrade and fabrication (V2): Improved MGT performance, PCIe enumeration, compatibility with higher Serenity version

In House Module Design (Mimic) + wire bonding + Pull Testing:



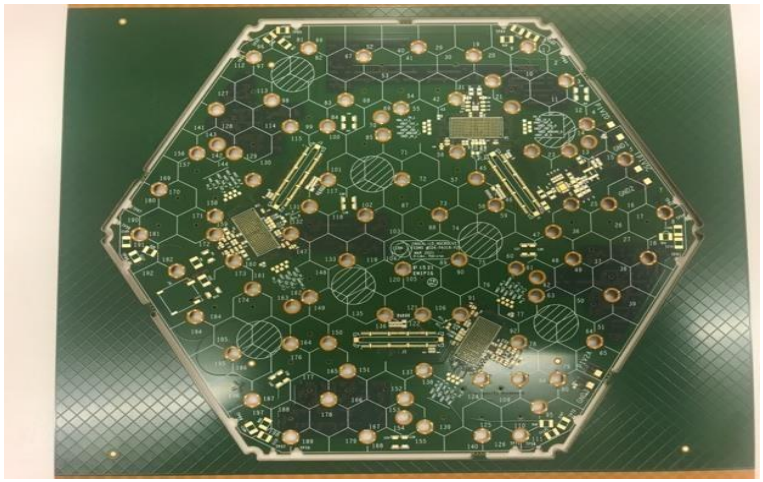


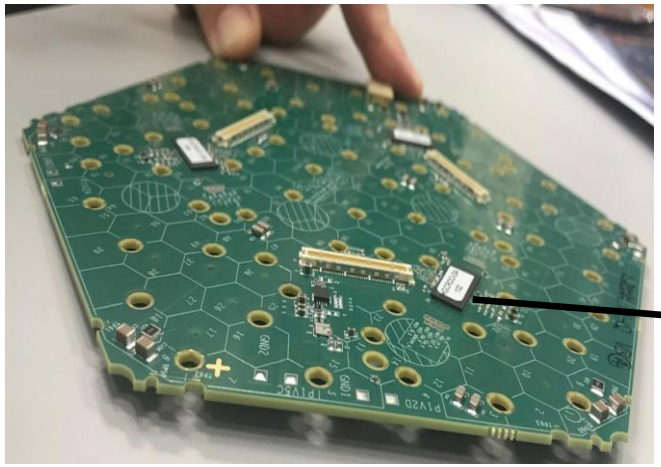


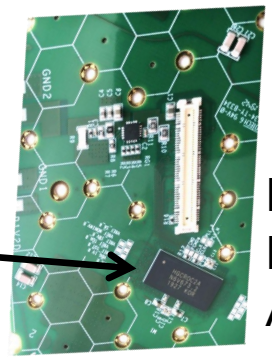


- Exercises of wire bonding and encapsulation, initially, on dummy stepped hole Hexabaord Module which would mimic the final Hexaboard along with Silicon sensor pad geometry.
- Two PCBs: Stepped Hole design with copper pads at 120°(4 layers) + Sensor pad geometry design (2 layers) ,then, make sandwich of twos with no flow prepeg.
- Fabrication of Stepped Hole design is challenging, tricky, not regular production job.
- M/s. Micropack offered cost effective solution
- V1: Alignment offsets in stepped holes with Sensor PCB + prepeg dispersant issues.
- Work hard to technically guide (stackup thickness, dielectric (High Tg + Hallogen Free)) with Micropack to mitigate the issues
  V2: offset nullified, spread of no flow prepeg was quite restricted.
- Exercises: Wire bonding exercises and encapsulation

Fabrication and Assembly of NSH (Non stepped Hole) Hexaboards:

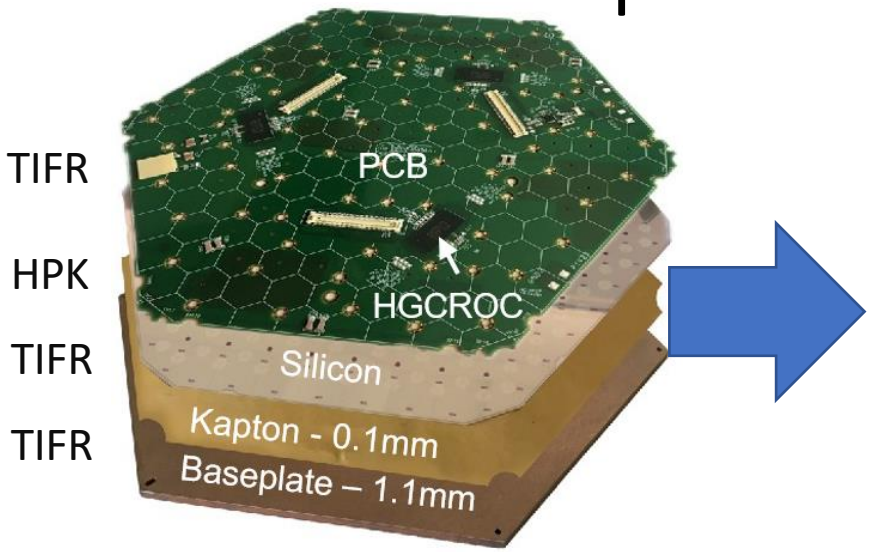


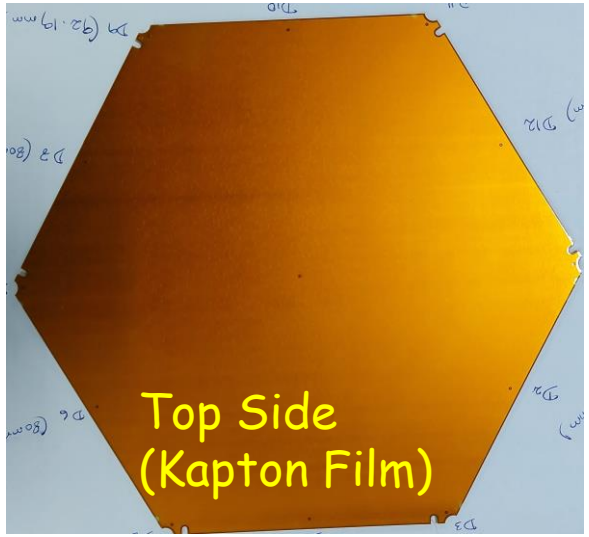


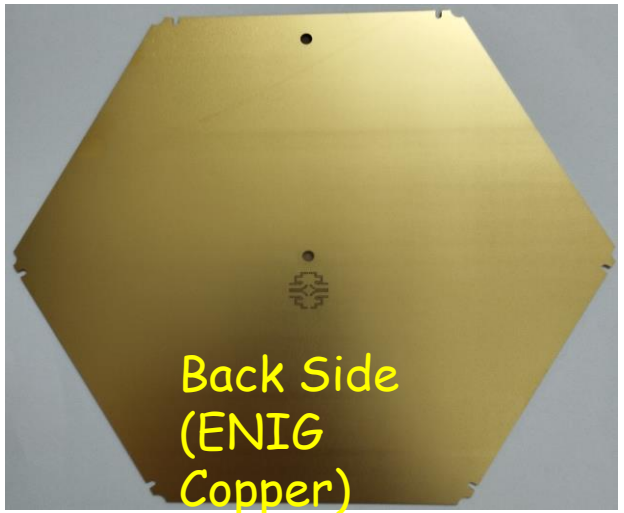


- To ascertain technical capabilities of the Indian PCB industry to fabricate the stepped hole Silicon Module design, NSH board (LD version) (litmus test?) were offered to them.
- Design: Class-3, HDI,
  - 1.2 mm thickness, 8 layers and multiple micro-via pairs
  - µBGA HGROC package (0.6mm pitch)
  - Tight impedance control signals (differential line geometry) and signal integrity verification
  - ~2400 Backdrills
  - No Stepped Holes (Only through holes)
  - Dielectric >Mid Tg and Hallogen Free (limited Range)
  - Twist < 0.75% (!>1.4mm)
- Two PCB Industry leaders, Hi-Q and Micropack proposed. (>7 fabricators were contacted). Hi-Q won (cost effective solution.
- Worked hard with Hi-Q to provide minute technical clarities (during pre-engineering stage) present in the design to ascertain that design reaches to its production level
- Two out of Ten Fabricated PCBs were taken for initial QC (flatness, twist/warp etc.). Eight were sent to concerned group at CERN
- At CERN, some of the PCBs assembled. Twist got almost doubled during assembly. Needs Investigation
- As per Hi-Q, dielectric material (TU-862HF) could be probable candidate for higher (past experience)

PCB Baseplates + Kapton:







First two Components of Si Module (Baseplate(PCB) + Kapton Film) (Thickness = 1.2mm, Tolerance ~ +/- 0.1 mm)

Modules with PCB Baseplate: CE-E and low Rad. of CE-H

Mounting platform for the Si sensor and Frond End PCB (Hexaboard) on Cassettes

Blind Hole and Blind Slot (0.8mm - nonconical) to mount on the Cassettes, Tight Tolerances ~ +/- 50µ (achieved)

Kapton film for biasing the sensor backplane and insulation

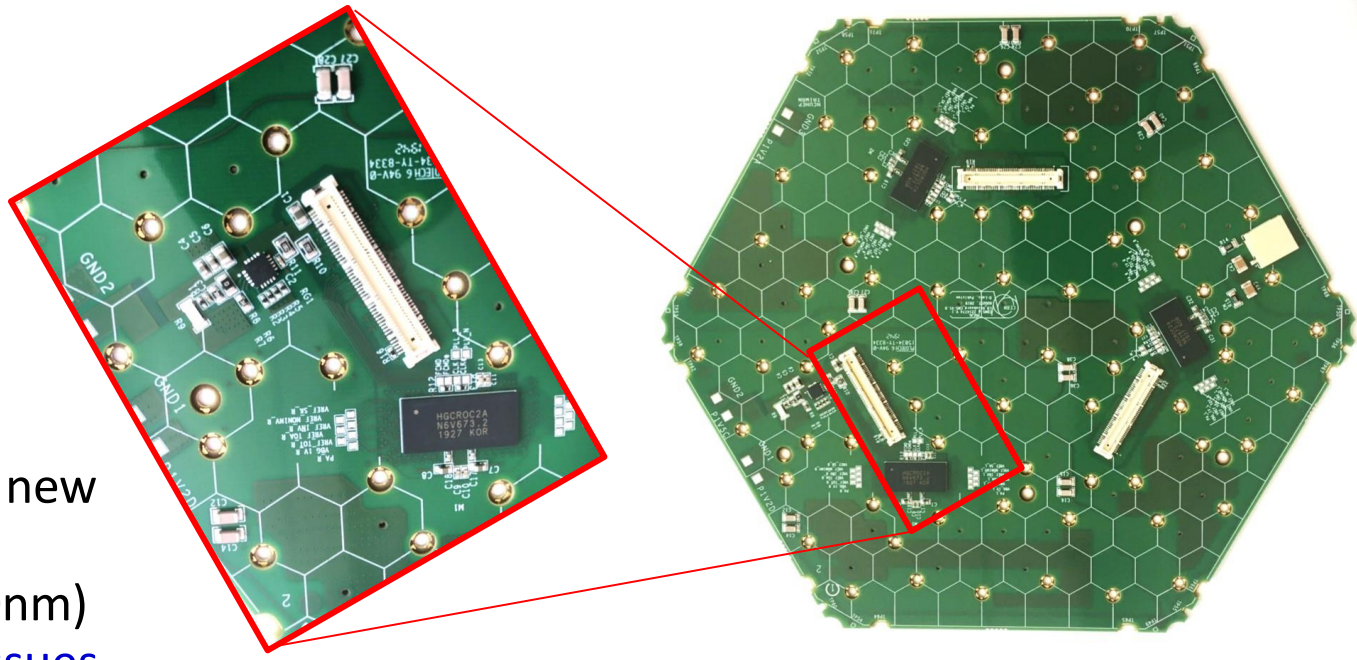
Three types of Fiducials on Top to align and mount Sensor + PCB

Hi-Q : 20 PCBs, Micropack: 20 PCBs

Extensive QA/QC measurements: by Mukund (Separate Poster)

Our R&D efforts with these two PCB Industry leaders could register them to take participate in the Global Survey of HDI PCB fabrication (Frontend + Backend) for the HGCAL

Next steps:



V3_LD_V1.2 full hexaboards

- Same stackup as NSH boards but:
  - Include the stepped holes!
  - Made for LD-packaged HGCROC-V3
  - Same Design as NSH
  - Our R&D efforts with Hi-Q led us to device a new technique of developing Stepped Holes
  - This technique requires only Co2 laser (9600nm) drilling and plasma cleaning (no alignment issues, no dispersant of prepeg)
  - Will confirm this technique in TIFR on PCB test coupons
  - Awaiting Two Sample PCBs from HI-Q and one from Micropack – This week!!

Cu/W Baseplates:

- Cu/W baseplates in pipeline
- Cu/W sheets cutting in Hex shape (Mousebite + Notch) @ TIFR (Jet Cutting?)
- Sample of (100mm x 100mm) Cu/W sheets procurement started

Thank You