CMVD Frontend
DHEP Annual Meeting 2022
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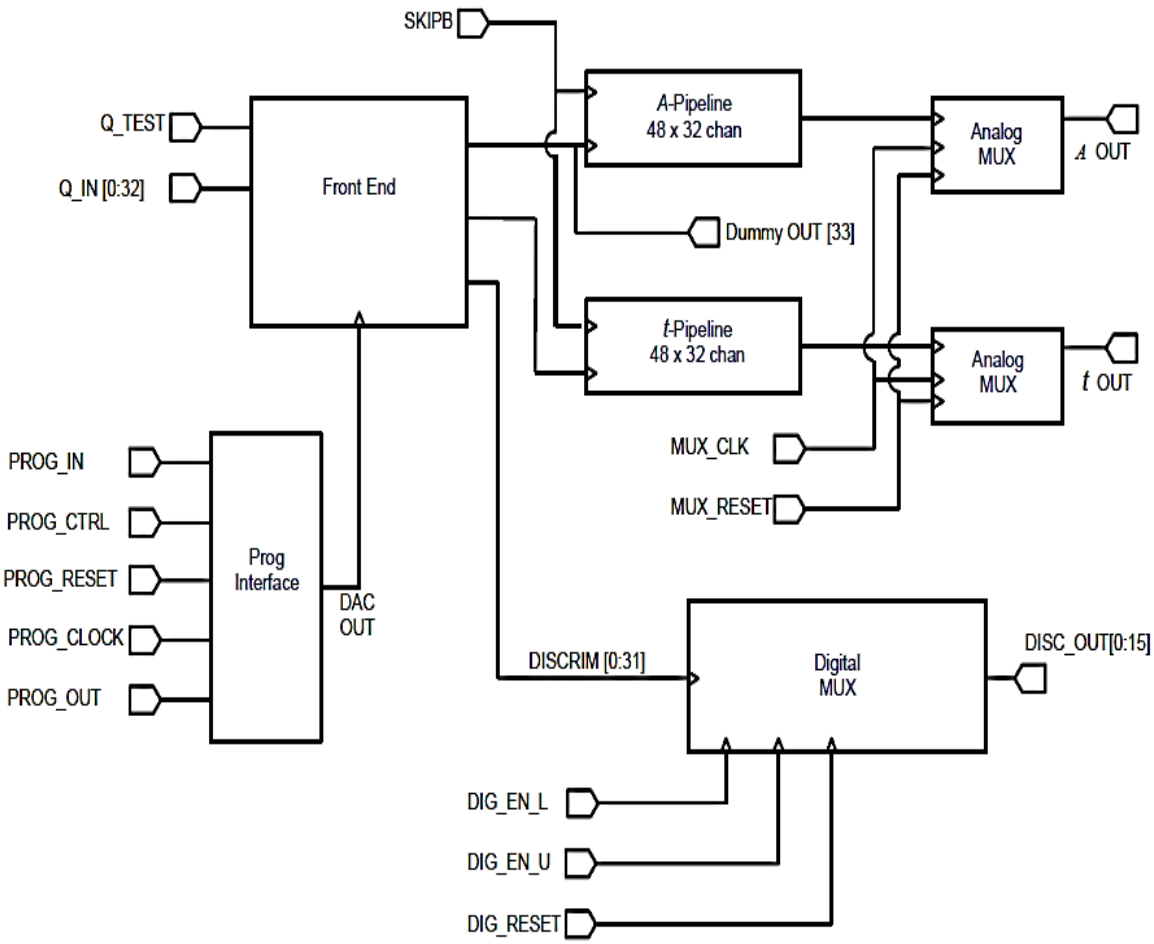
Contents

1. DAQ Requirements for CMVD
2. Trip-T
3. VMM3a
4. WEEROC chip Comparison
5. Citiroc based Front end Design and preliminary results
6. DRS4 based Front end Design and preliminary results
7. Future plan

Features	CMVD DAQ Specifications
Channels	64 or 32
Polarity	Positive
Detector	SIPM S13360-2050VE
HV Trimming	Range ~1V
Architecture	LG Charge, HG Charge and Timing
Amplifier gain	Reasonable gain
Shaper peaking time	Tunable to capture Peak amplitude
ADCs	12 bit
Charge Dynamic range & resolution	50pC , 0.04pC
Timing resolution	100ps – 150ps
Multiplexed Analog out	Required if external ADC needed
Trigger Out	ToT or ORed Time or charge trigger
Readout	Reasonable (Dead time :100us)
Detecting method	Capturing and digitizing of CMVD signals on RPC stack muon trigger.
LG, HG and TAC	At least 32 channel LG charge, HG charge and Timing from one card.

TRIP T Front End

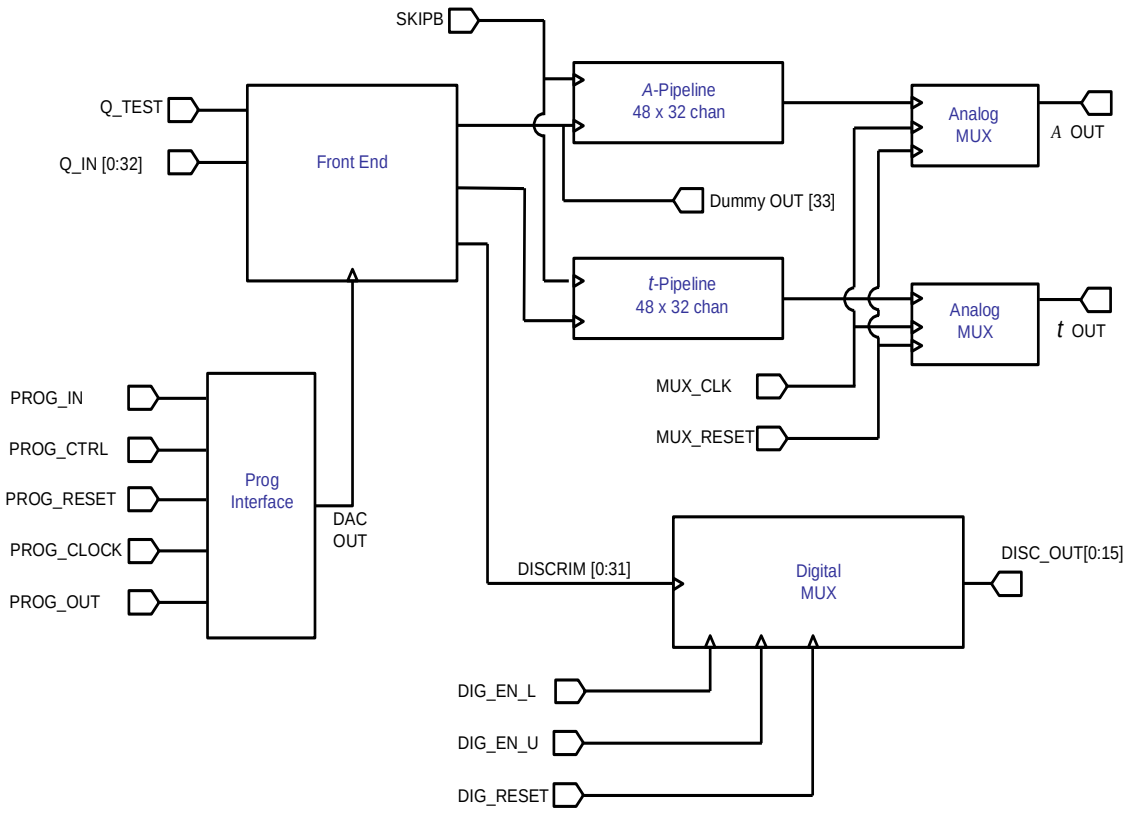


Features:

- 32 channel charge amplifier
- Charge and time of arrival output per channel
- 48 depth Analog pipeline storage per channel for both parameters
- 16 digital outputs crossing set threshold at a time
- Multiplexed valid channel readout
- Common Test pulse for calibration

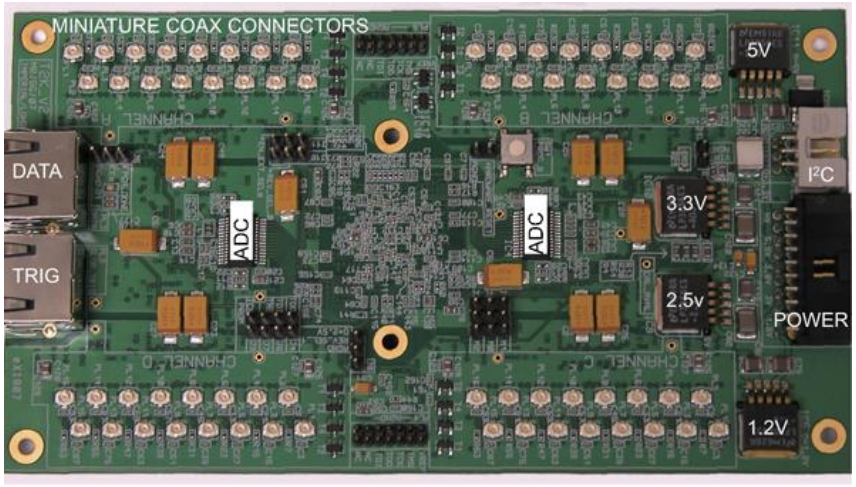
Trip-t chip designed by Prof. Abderrezak Mekkaoui for D0 FE electronics

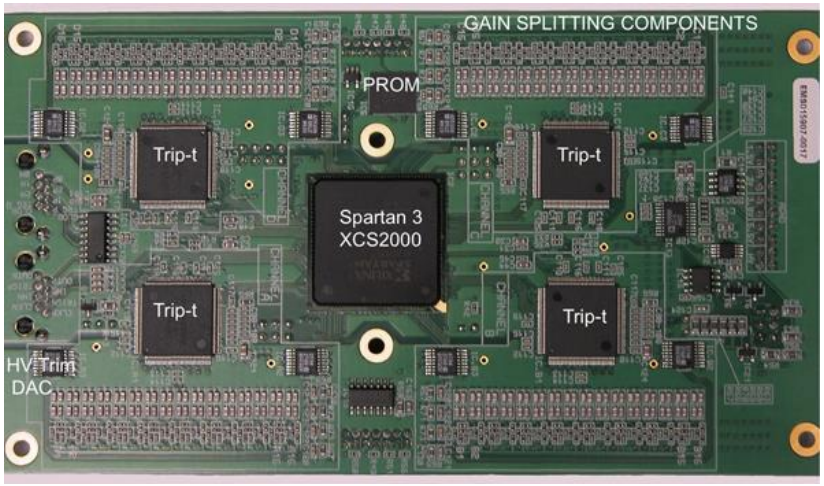
TRIP T Front End

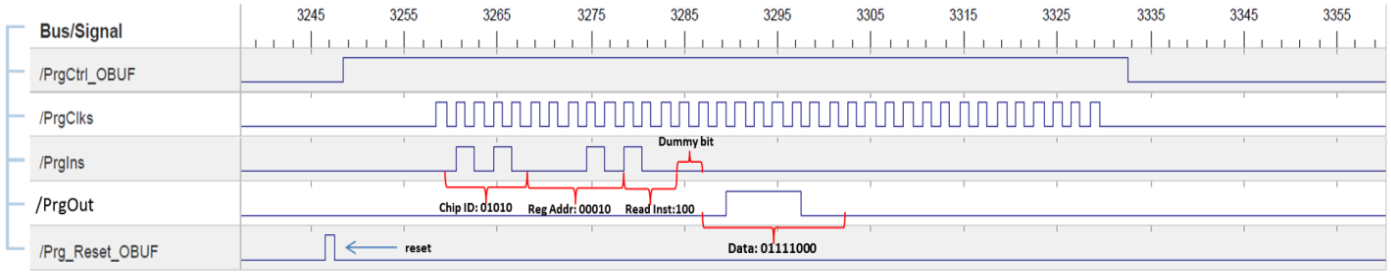


- 32 Channel charge amplifier
- Charge & time of arrival o/p per channel
- 49 deep analog pipeline storage per channel for both parameters
- 16 digital o/ps crossing set threshold at a time
- Multiplexed valid channel readout
- Common test pulse for calibration

TFB Module designed for T2K ND280 Detector Readout



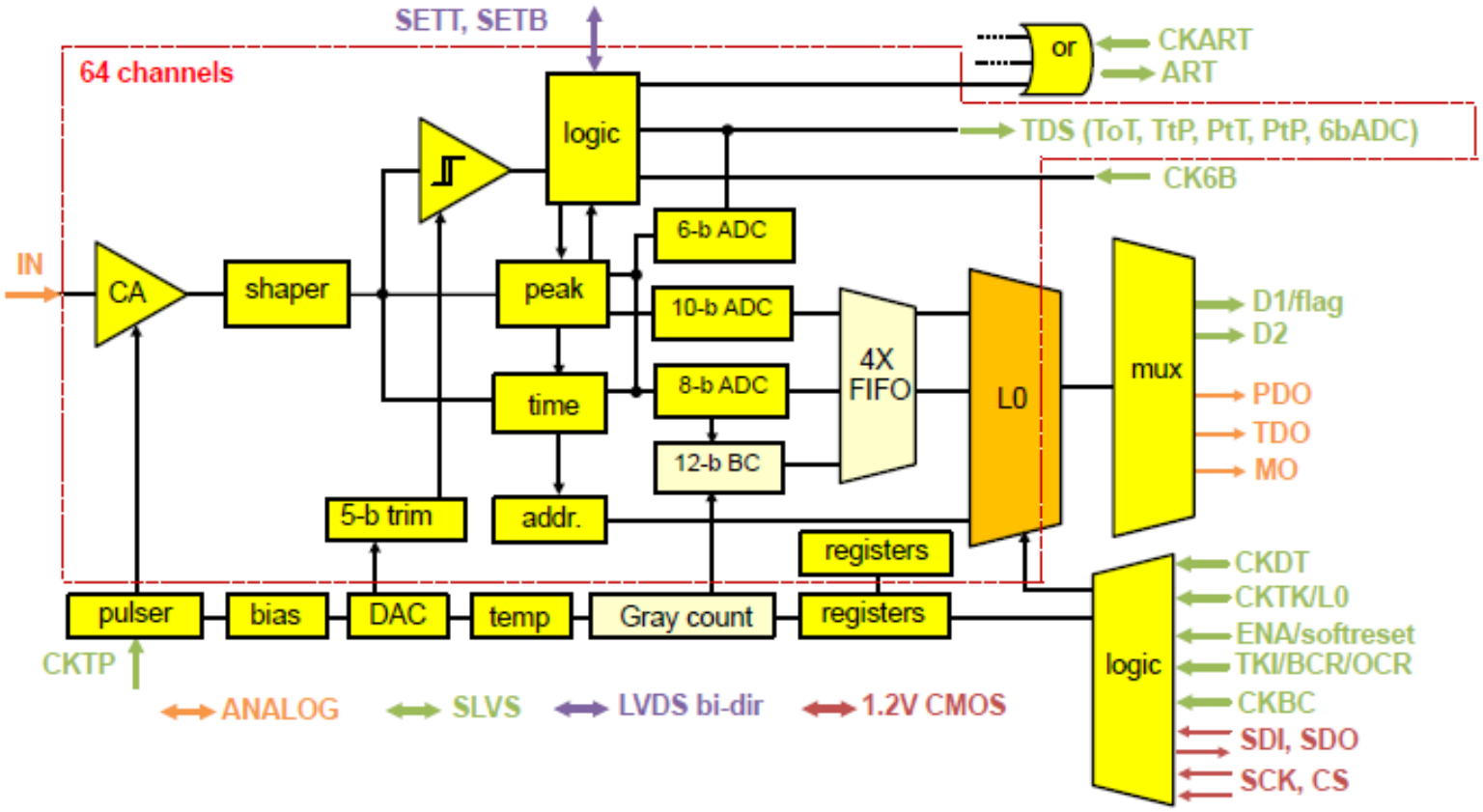


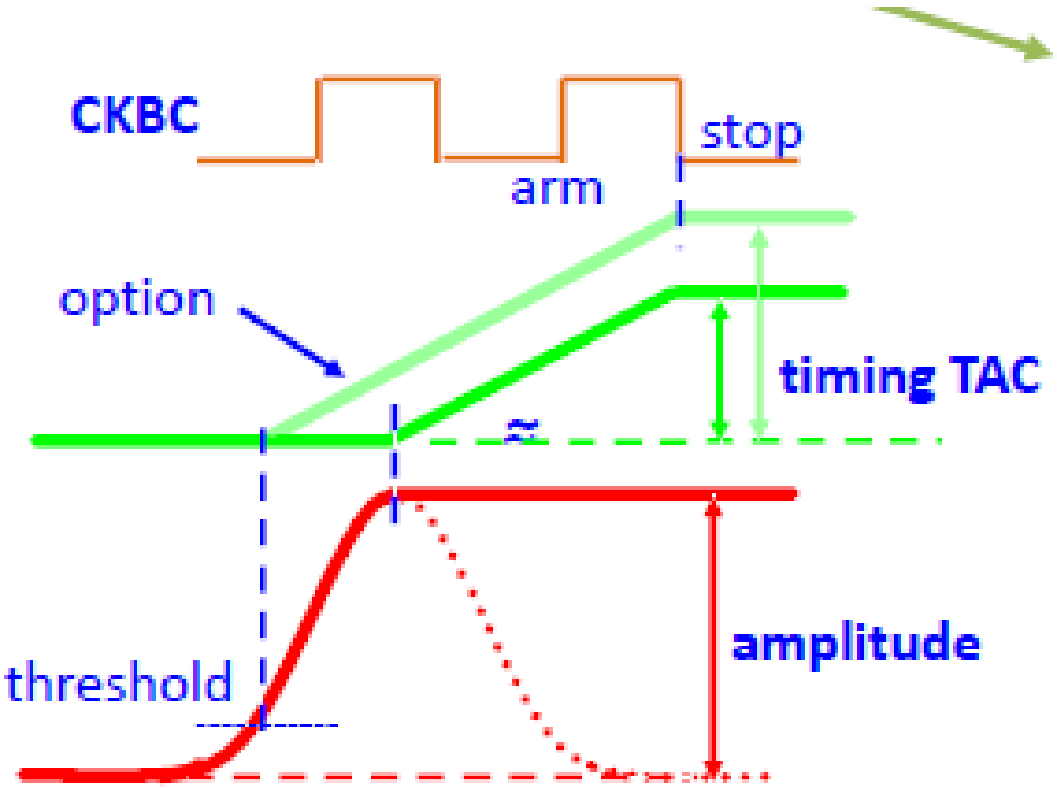


Control Register access using chip scope

Due to lack of technical support for Trip T we stopped pursuing further.

VMM 3a ASIC


SETT, SETB
64 channels
or
CKART
ART
logic
TDS (ToT, TtP, PtT, PtP, 6bADC)
CK6B
6-b ADC
IN
CA
shaper
peak
10-b ADC
4X
FIFO
L0
mux
D1/flag
D2
time
8-b ADC
PDO
TDO
MO
12-b BC
5-b trim
addr.
registers
pulser
bias
DAC
temp
Gray count
registers
logic
CKDT
CKTK/L0
ENA/softreset
TKI/BCR/OCR
CKBC
SDI, SDO
SCK, CS
CKTP
ANALOG
SLVS
LVDS bi-dir
1.2V CMOS



- Programmable Input polarity
- Input capacitance sub-pF to nF
- Gain: 0.5,1,3,4,5,6,9,12,16 mV/fC
- Shaper along with Baseline restorer
- Adjustable Peaking time
- 25,50,100 and 200ns
- Discriminator Threshold programmable using 10 bit DAC
- Peak Amplitude detection
- 200ns Dead time once a peak found
- **10 bit ADC for Peak amplitude**
- TAC Ramp Duration :
- 60ns,100ns,350ns,650ns.
- **8 bit ADC for timing measurement**
- 6 bit ADC for logic for triggering

Three Modes of Readout

1. Two Phase analog Mode
2. Continuous or Continuous + Ext trigger mode
3. L0 mode

But this chip covers only a dynamic range of 2pC which is not sufficient for CMVD requirement.

WEEROC Chips

Features	Citiroc 1A	Petiroc 2a	Triroc 1A
Channels	32	32	64
Polarity	Positive	Positive or negative	Positive or negative
Detector	SIPM,RPCs	SIPM,RPCs	SIPM
HV Trim	8bit DAC ~2.5V or 4.5V range	8bit DAC ~1V (4mV res)	8bit DAC ~ 2.2V
Architecture	Amplifier, LG Amplifier & CR-RC Shaper, HG Amplifier & CR-RC Shaper, Fast Shaper for Trigger	Amplifier, LG CR-RC Shaper, SCA/ Peak detector, TAC, ADCs	Amplifier, LG and HG CR-RC Shaper, SCA/ Peak detector, TAC,ADCs
AMP gain	Programmable for HG and LG amplifier using 6 bit DAC	Fixed gain 40	13mV/p.e positive 16.5mV/p.e negative
Shaper peaking time	Adjustable 12.5ns to 87.5ns (resolution 12.5ns)	Adjustable 25,50,75 100 ns	Adjustable 10ns to 1.28us (10ns res)
ADCs	No ADC, External ADC	10 bit – Peak or SCA 10 bit - TAC	10 bit – Peak or SCA 10 bit - TAC
Charge Dynamic range & resolution	160 fC - 400 pC i.e. 2500 pe	0-480 pC i.e. 3000 pe	HG : 100 pe, LG : 3000 pe,
Timing resolution(With 40 MHz ref clk)	No Timing, External TDC	100 ps	88 ps

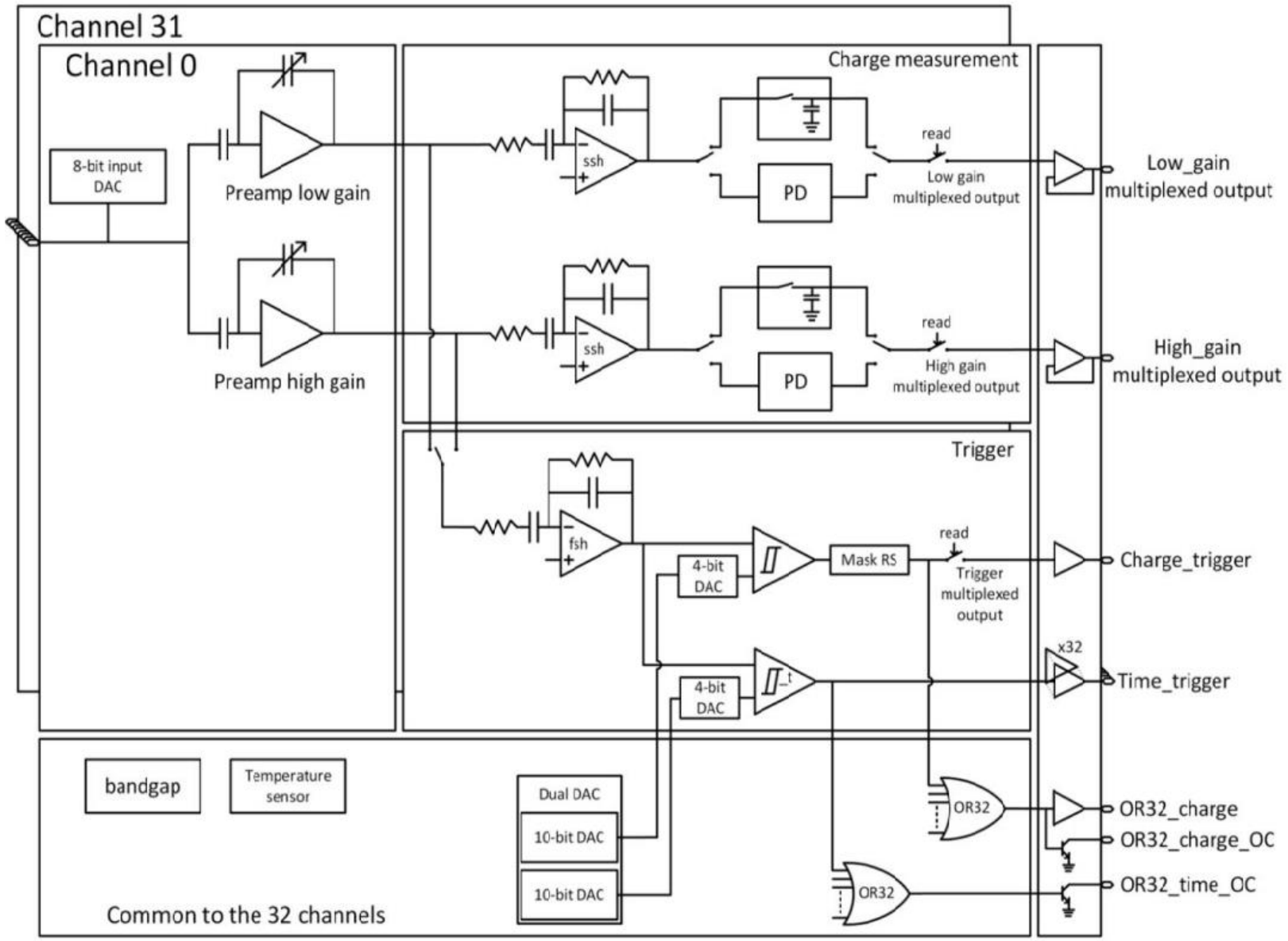
Multiplexed Analog out	**LG Peak or SCA HG Peak or SCA**	**LG Peak or SCA out**	**LG (Peak or SCA) , HG (Peak or SCA) and TAC,**
Trigger Out	**Disc out all 32, Charge NOR32, Time NOR32**	**Disc out all 32, Charge OR32, Time OR32**	**Time trig ch, Charge OR64, Time OR64,**
Package	**TQFP160 – TFBGA353**	**TQFP208 – TFBGA353**	**BGA (12x12mm, 353 balls)**
Readout	**Multiplexed Analog out**	**1 line serial at 160MHz**	**4 line serial at 160MHz**
Detecting method	**Local trig using 32 ch Disc out and issue hold signal when RPC trigger and local trigger matches**	**Local trig using 32 ch Disc out and issue hold signal when RPC trigger and local trigger matches**	**Issue Hold signal when RPC trigger comes, Note: shapers peaking time to be set close to RPC trigger latency.**
LG,HG and TAC	**32 Ch LG charge 32 Ch HG charge**	**32 Ch LG charge INT ADC, 32 CH TAC INT ADC.**	**LG 64 ch charge INT ADC , HG 64 Ch TAC INT ADC and MUX HG charge (peak or SCA) EXT ADC**
Price	**-**	**28650 each+18% or 5 % GST(100 Qty)**	**RS. 48000 each + 18% or 5 % GST(50 Qty) RS. 40820 each + 18% or 5 % GST(100 Qty)**

Citiroc doesn't have internal ADCs but consist of separate LG and HG path

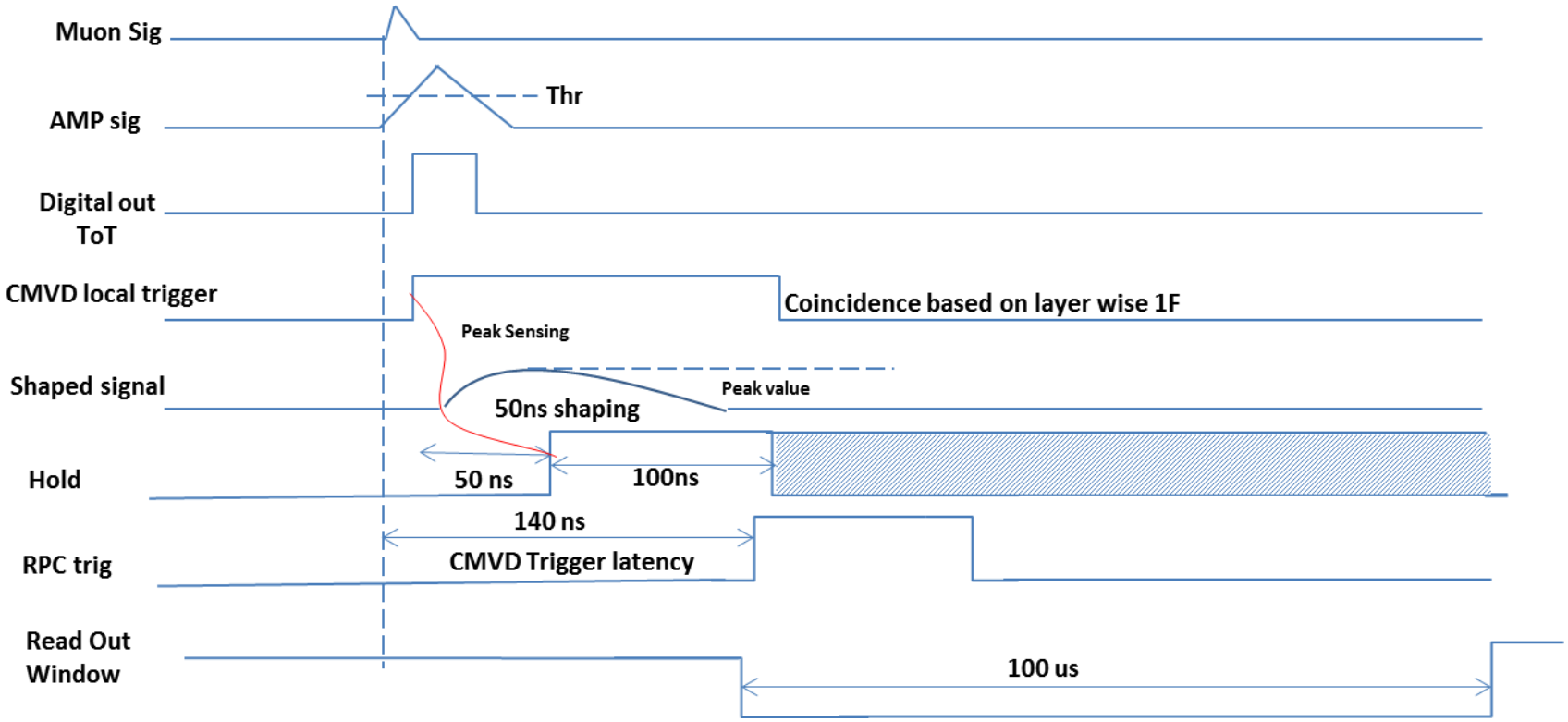
Petiroc doesn't have separate high gain and low gain path.

Triroc doesn't have dedicated discriminator outputs. No local trigger.

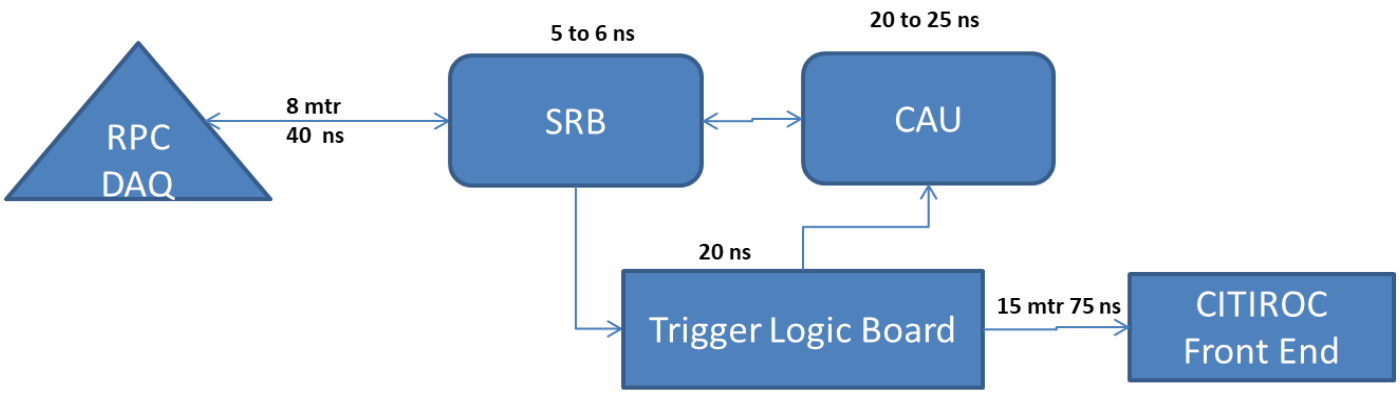
Citiroc 1A


Channel 31
Channel 0
8-bit input DAC
Preamp low gain
Preamp high gain
Charge measurement
ssh
PD
read
Low gain multiplexed output
High gain multiplexed output
Low_gain multiplexed output
High_gain multiplexed output
Trigger
fsh
4-bit DAC
Mask RS
Trigger multiplexed output
Charge_trigger
x32
Time_trigger
bandgap
Temperature sensor
Dual DAC
10-bit DAC
10-bit DAC
OR32
OR32_charge
OR32_charge_OC
OR32_time_OC
Common to the 32 channels

CITIROC timing and Latency requirement



CMVD Trigger = 40 + 5 + 20 + 75 = 140 ns



Testing of Citiroc using A1702/DT5702 module

-33mV

Discriminator

P1

P2

P3

Linear FIFO

F1

F2

F3

F4

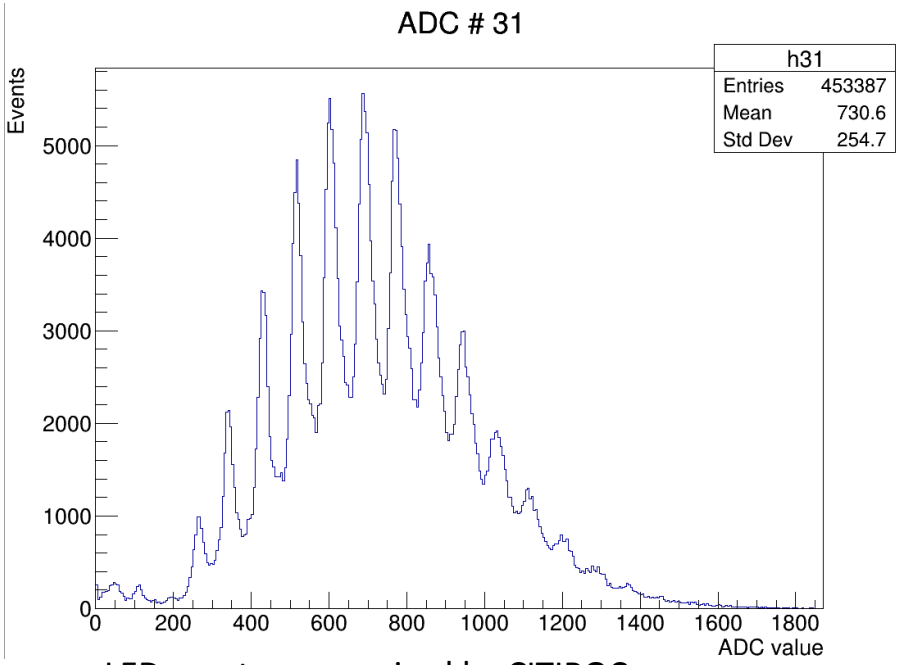
S1

DT5702 Citiroc Module

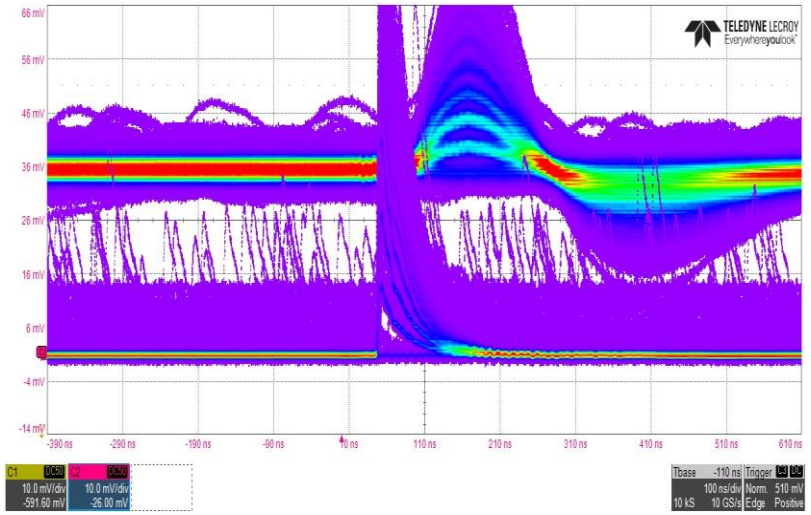
Global Trigger

Scaler

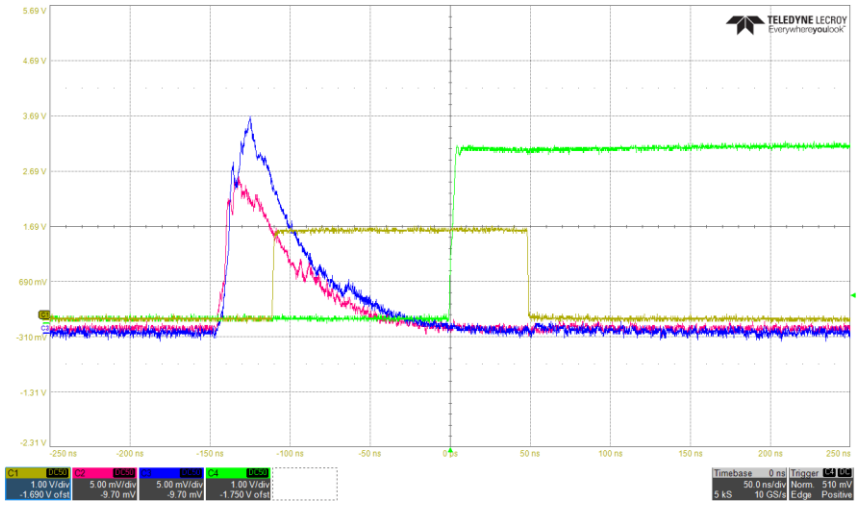
Setup done by Raj Shah



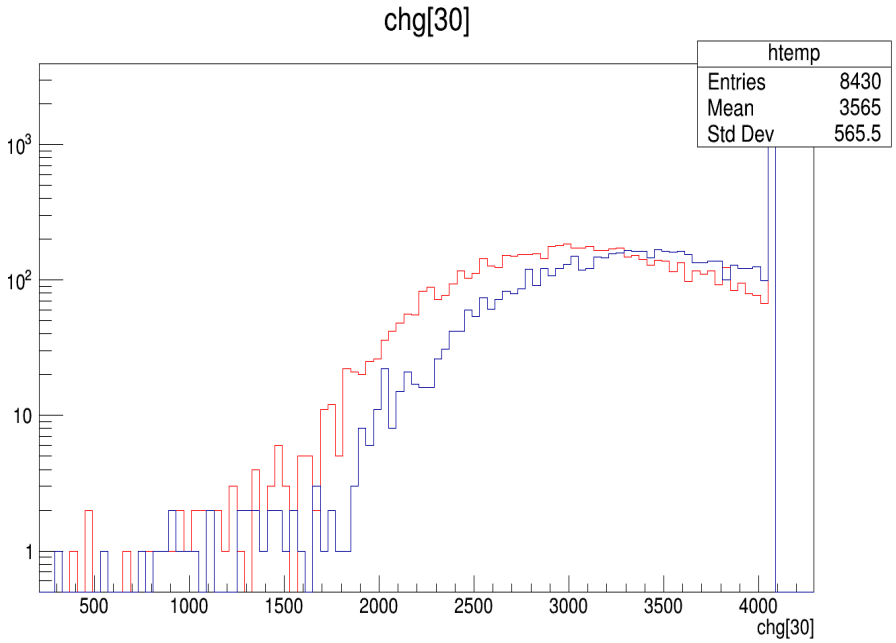
LED spectrum acquired by CITIROC



High Gain Shaper response of Citiroc with LED source



Typical Trigger logic and DAQ response



Acquired ADC response of one of the HG channel in Cosmic muon test

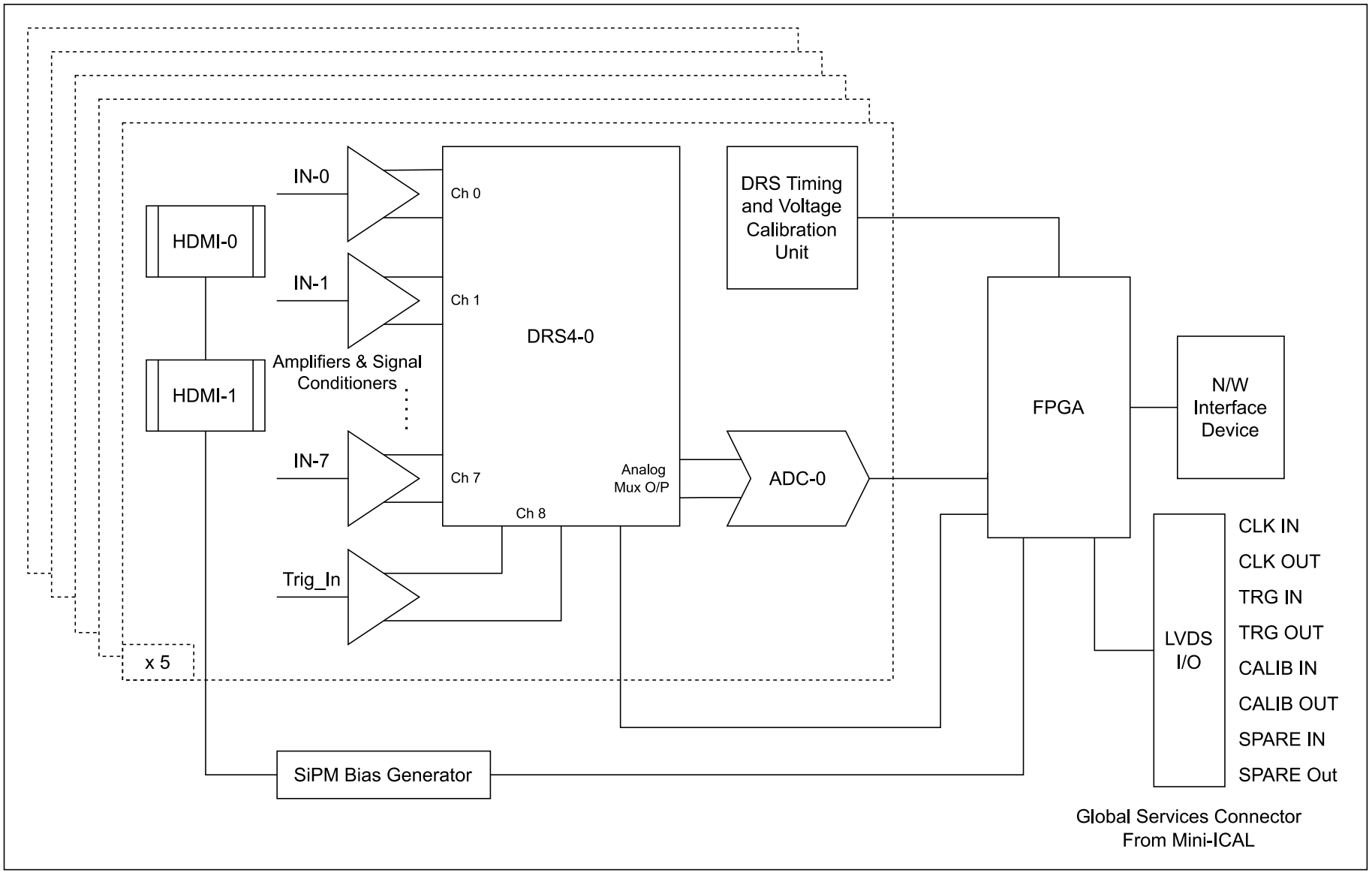
DRS4 Usability

- Pulse Time : 150 ns
- Sampling Time before pulse : 50 ns
- Overhead 100 ns
  - 30 ns jitter because of 5m long Scintillator/Fibre
- Total Sampling time : 300 ns

- Muon signals from SiPM have rise time of 5-10 ns
- Thus DRS4 sampling rate of 1 GSa/s is sufficient
- 1024 Samples at 1 GHz Sampling clock gives us 1.024 µs history
  - This is greater than 285 ns trigger latency + 300 ns sampling time
- Input signal range up to 1 V, at a gain of 1200 ohm

- DRS4 sampler is suitable in terms of timing and signal amplitude

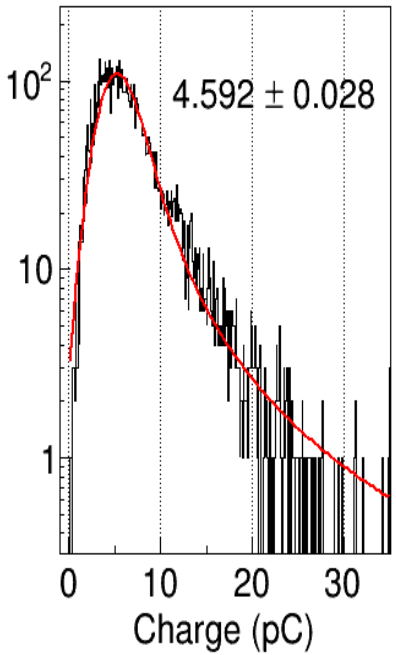
DRS4 Based SiPM Data Acquisition Board

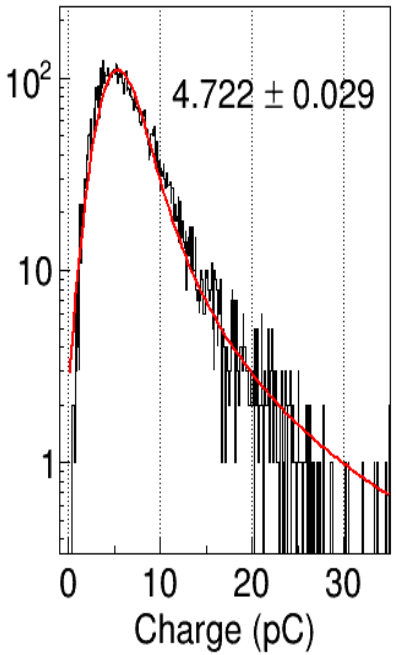


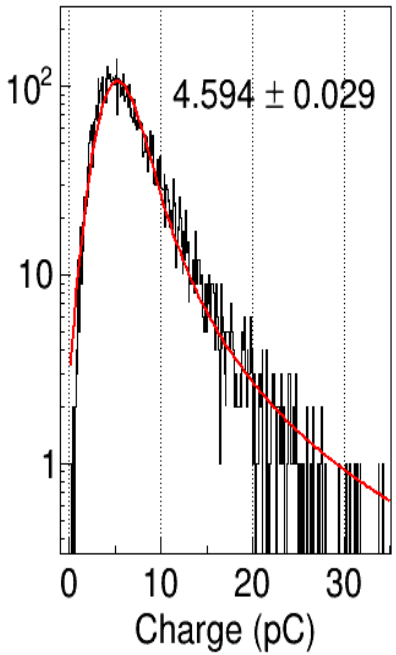
Data Throughput Calculation for a single DAQ Board after ZS

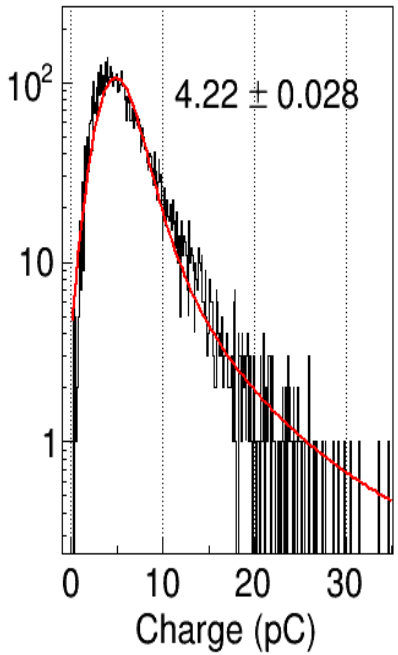
- Assuming a) ZS is active, b) CM is inactive
- Rejecting all noise pulses leaves only muon pulses
- The max occupancy rate for a scintillator is 15 Hz
- In a CMVD DAQ board we have 40 SiPMs
- We need to record the pulse profile for at most 300 ns
- For 1 GHz sampling frequency, 300 ns converts to 300 samples. Also we have ADC of maximum 16 bits (2 bytes).
- Thus data rate can be calculated as:
  - $Data\ Rate = 40\ SiPMs \times 300\ samples\ \times 2\ bytes \times 15\ Hz$
  - Thus maximum data rate shall be 360 kBytes/s OR 3.6 Mbits/s
- Data rate of 3.6 Mbps is easily sustainable with Wiznet W5300 + NIOS II combination

Dicounter Testing using DRS4

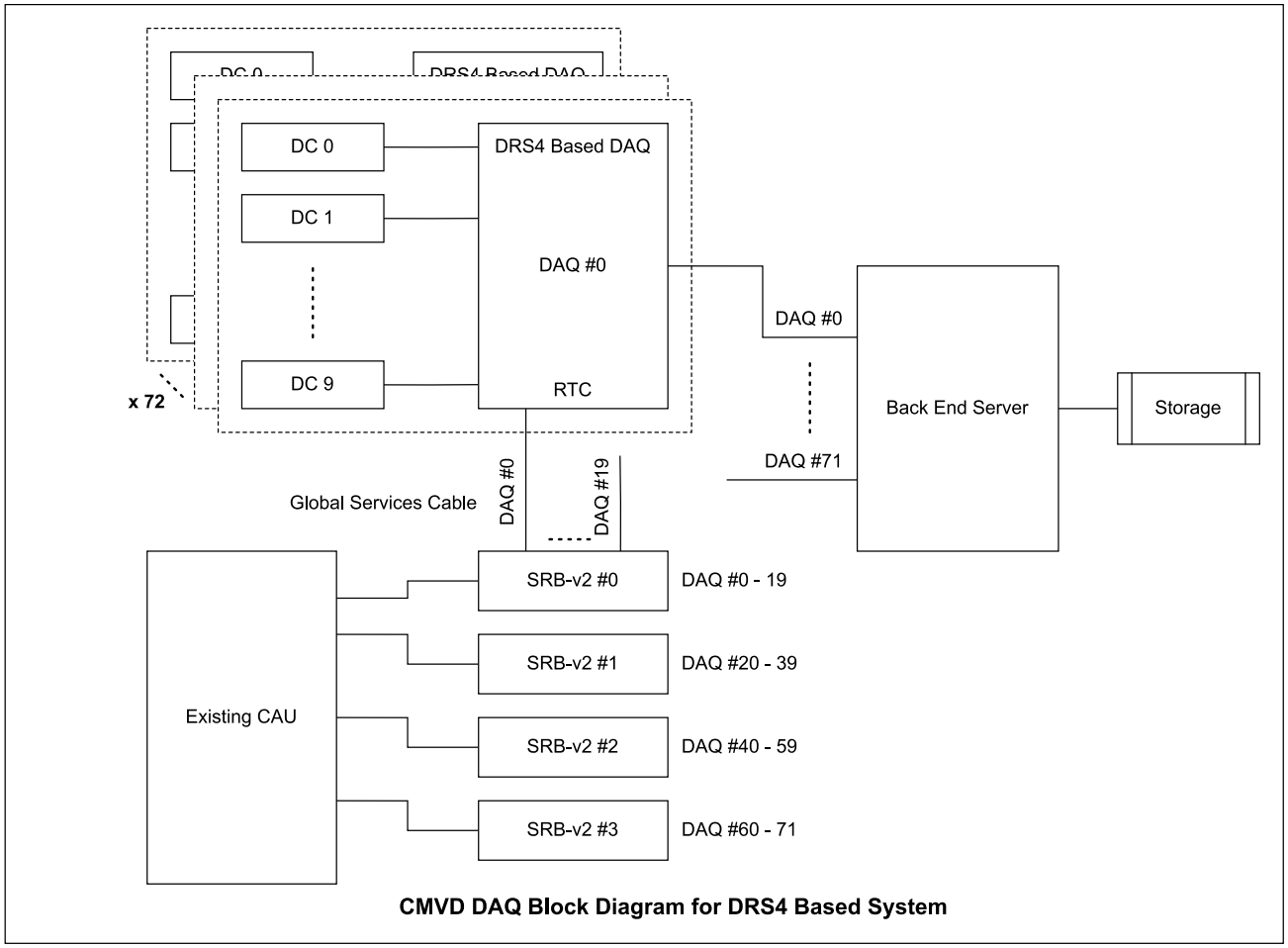




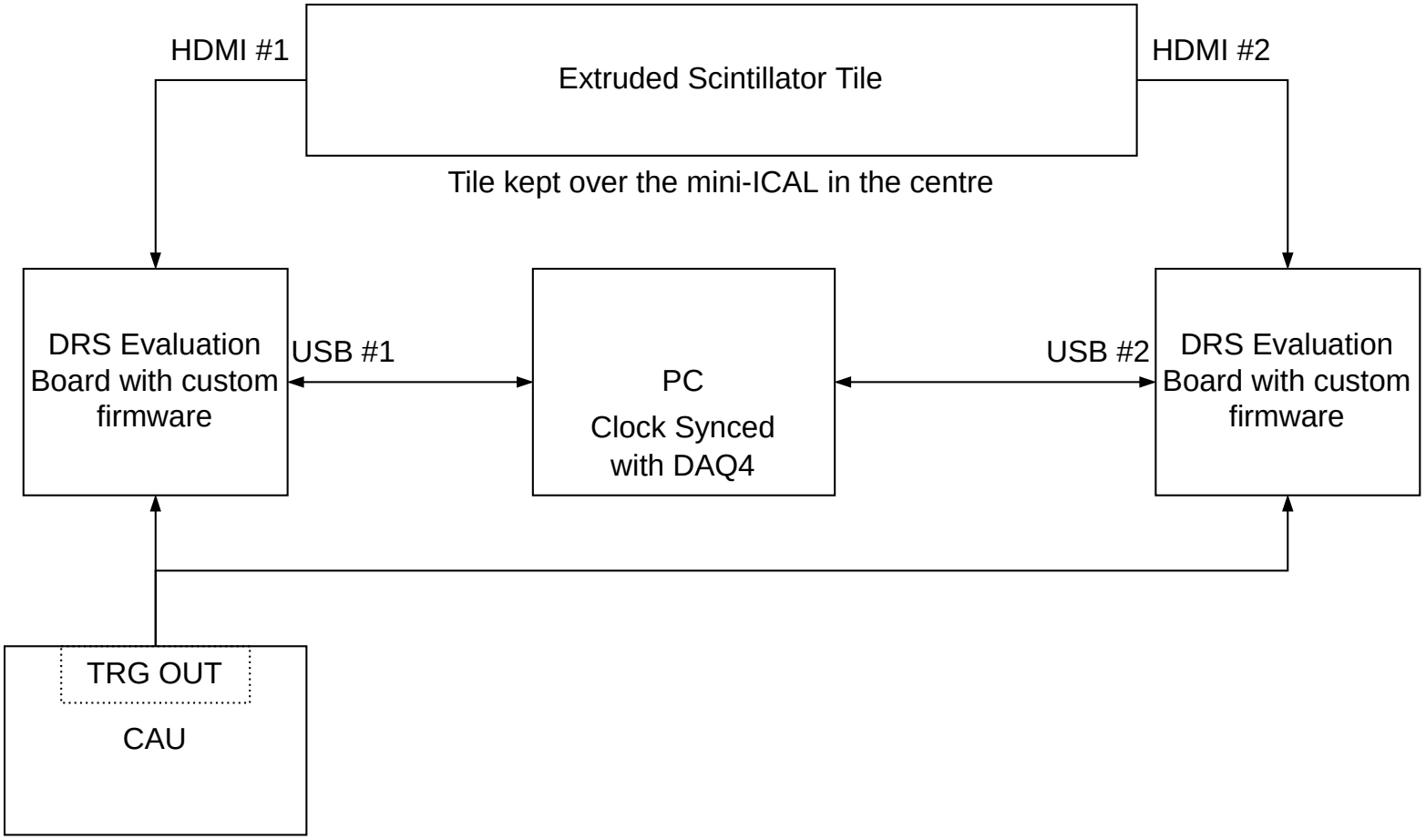




CMVD DAQ System Block Diagram



Prototyping with the mini-ICAL



Immediate action

1. Decision to use DRS4 or Citiroc 1A based on results
2. FE prototyping including SiPM bias and LED calibration facility

Future plan

1. All subsystem development and Software design
2. Procurement of all components required for CMVD
3. Mass production and testing
4. Integration and Commisioning

Thank You