Application of Embedded System for High Energy Physics Experiments

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DHEP Annual Meeting

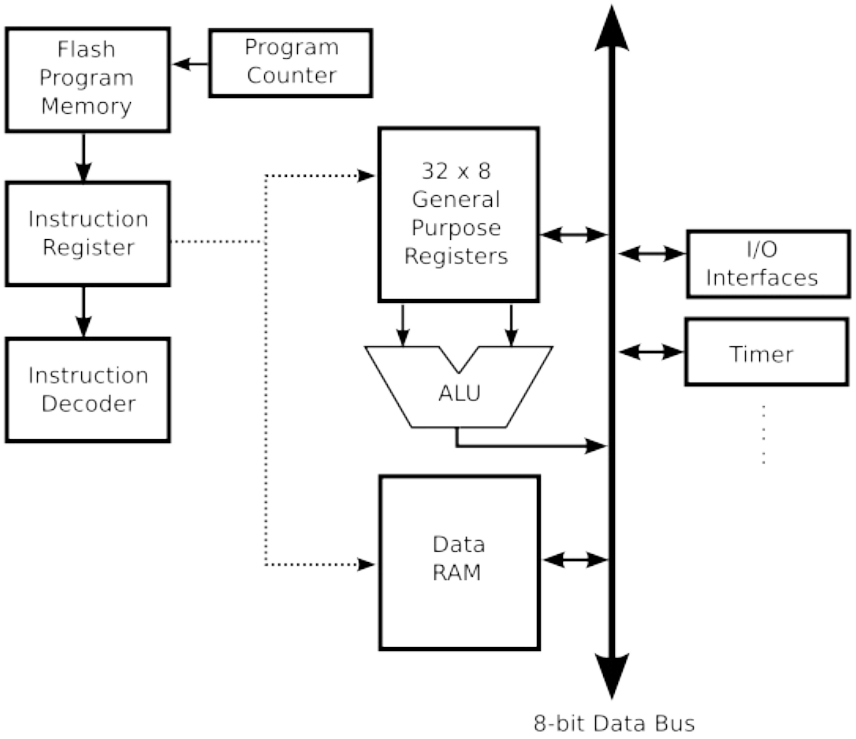
6th May 2022

Outline

- Evolution of Embedded Systems (ES)
  - Microcontroller, FPGA, …
- Applications of Embedded Systems to the GRAPES-3 Experiment
  - FPGA based high-speed scalar
  - Triggerless Muon DAQ System (TM-DAQ) for GRAPES-3 experiment
- Applications of Embedded Systems to the CMS Experiment
  - FPGA based GF-Radiation Monitoring Detector DAQ system
  - Trigger Primitive System for HGCAL Detector : Design and fabrication of high end FPGA based (VU7P) trigger primitive generation system for HGCAL detector
- Summary

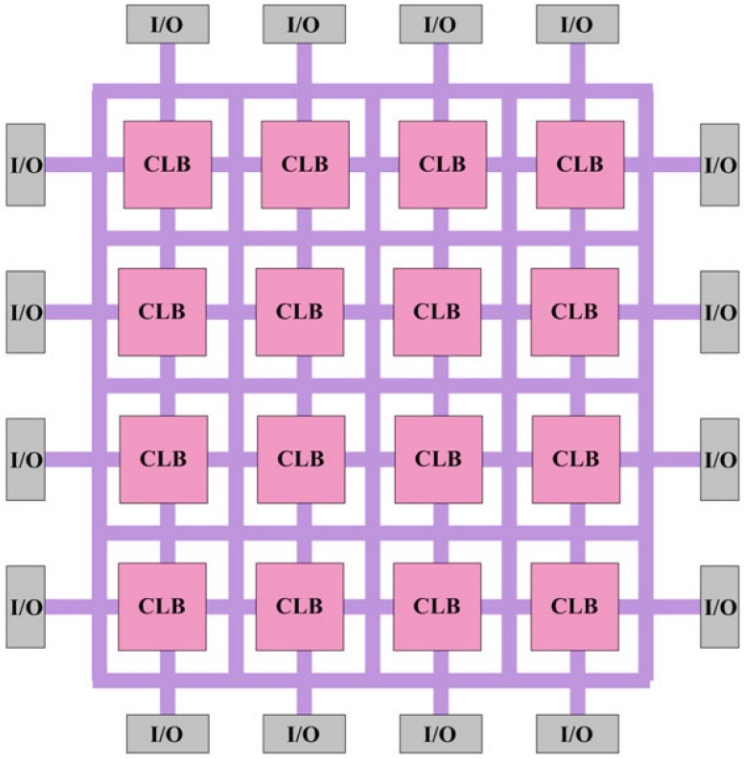
Architecture Micro-controller

- **High level code (like "c") are converted into ALU instructions (assembly language).**
- **This assembly program is stored into the program memory**
- **Instructions are executed one by one in ALU.**
- **Processes need to be scheduled to use the ALU (processing) resources.**
- **All serial operation**



Field Programmable Gate Array (FPGA)

- The most common FPGA architecture consists of an array of logic blocks, typically referred as Configurable Logic Block (CLB)
- CLBs are interlinked and linked to I/O blocks via complex connection matrix.
- Programming the FPGA creates a hand links between the logic blocks and I/Os.
- Many logic operation can happen simultaneously.



FPGA Design Flow

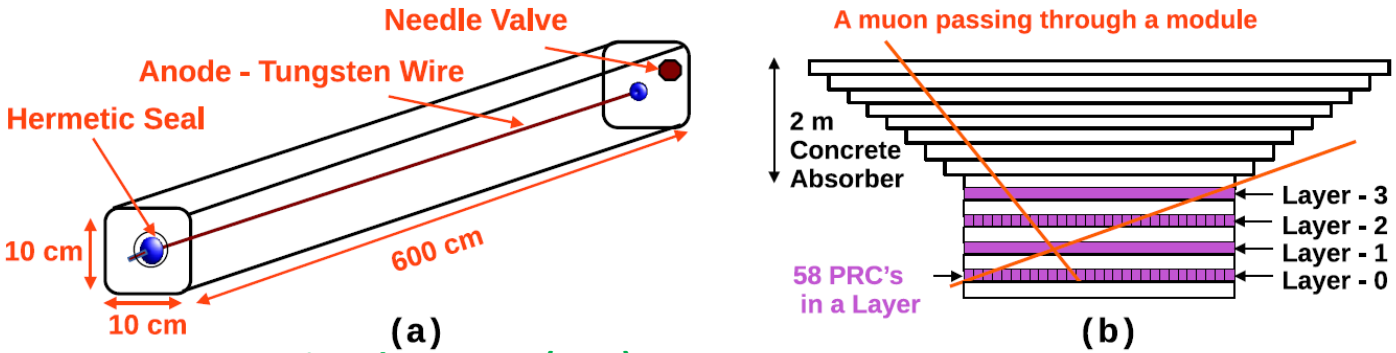
- Design Entry in HDL (Verilog/VHDL)
- Synthesis of the design into RTL schematic
- Complete design is broken into fundamental logic elements
- Implementation (mapping and routing)
- Generation of the memory map (programming file)
- Once FPGA is programmed with the map, the design is hardwired.

- Increase flexibility and performance of the FPGA many fold
- RAM (distributed and block)
- DSP blocks
- Encoders/Decoders
- Phase Lock Loop (PLL)\
- Operational Clock Frequency
  - Typically 100-250 MHz
- Communication Modules e.g. PCI, PCIe …

How complex systems can we build?

- Basic combinational and sequential logic circuits
- Memory controllers, display drivers ..
- High Speed communication interfaces: few Mbps to Multi Gbps
- Digital signal processors:
  - Complex high throughput video processing
  - Machine Learning
- Complex ASIC prototyping, Micro-processor inside FPGA
- System on Chip (SoC)
- And much more …We will discuss some of the cutting edge applications

GRAPES-3 Muon Detector



Proportional Counter (PRC)

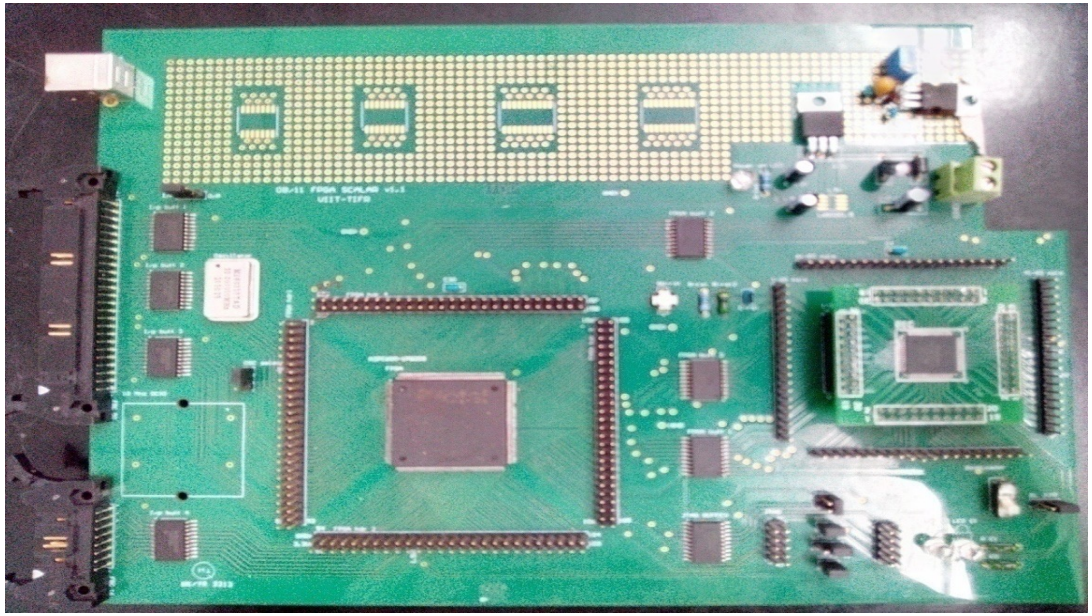
- Building block: Proportional counter (PRC) built during KGF era and still being used for last 35 years!
- Layer: Array of 58 proportional counters
- Module: Four Layers arranged in orthogonal layers
- Station: 4 Modules housed under single concrete structure
- Existing size: Four Operational Stations (576 m^2)
- Threshold: 1 GeV in a Vertical direction
- Muon Trigger: OR of 58 counters in a layer (Layer-OR) followed by AND of Layer-OR of each of four layer within 3 us
- Trigger Rate: 50 kHz (~4 Billion muons per day)

Muon Detector

High Speed 32-channel scalar

High Speed 32-channel scalar

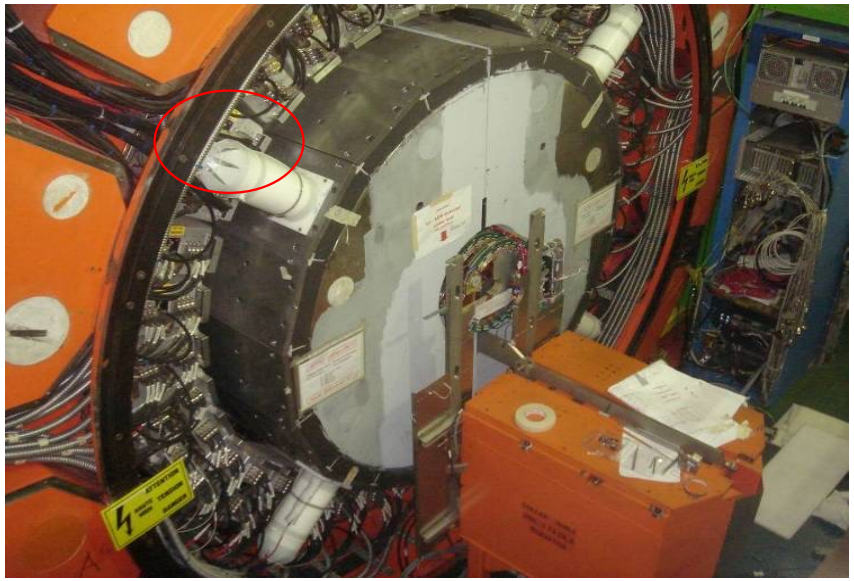
- **ACTEL PROASIC3E FPGA and a PIC18F87J50 microcontroller at heart.**
- **Very high speed (up to 10 MHz) and accurate counter.**
- **General Purpose FPGA development board.**



This embedded system has been used extensively for GRAPES-3 Proportional Counter testing (muon rate/pulse width measurement) including data data acquisition and many other applications..

DAQ for HF Radiation Monitor Detectors

HF Radiation Monitors

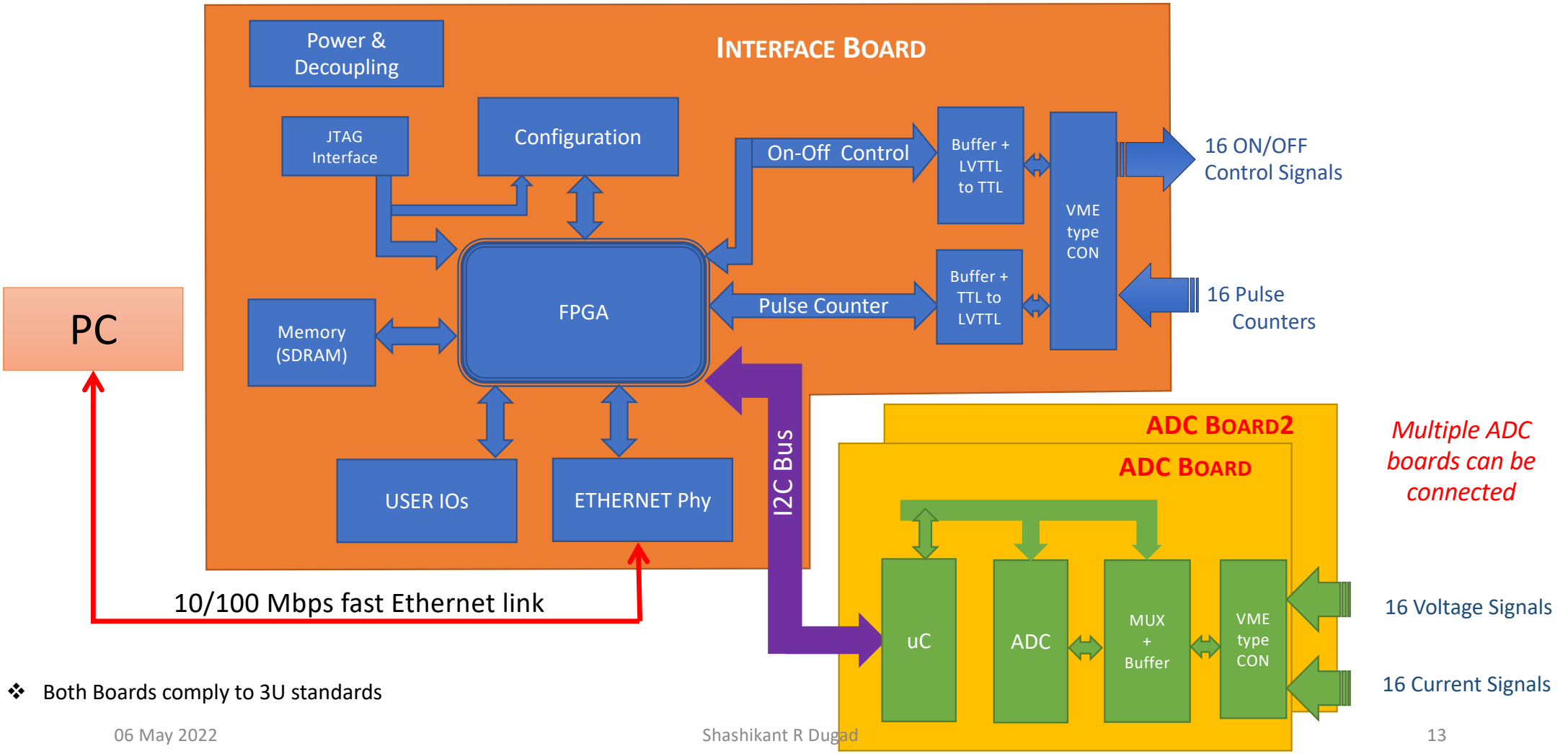


Objective of the monitors:

- ✓ **Long term monitoring of the absorbed dose and neutron flux to estimate the expected degradation of fibers, electronics, PMTs and to measure the shielding efficiency.**
- ✓ **Additional monitoring of the HF itself performance for future re-calibration etc.**

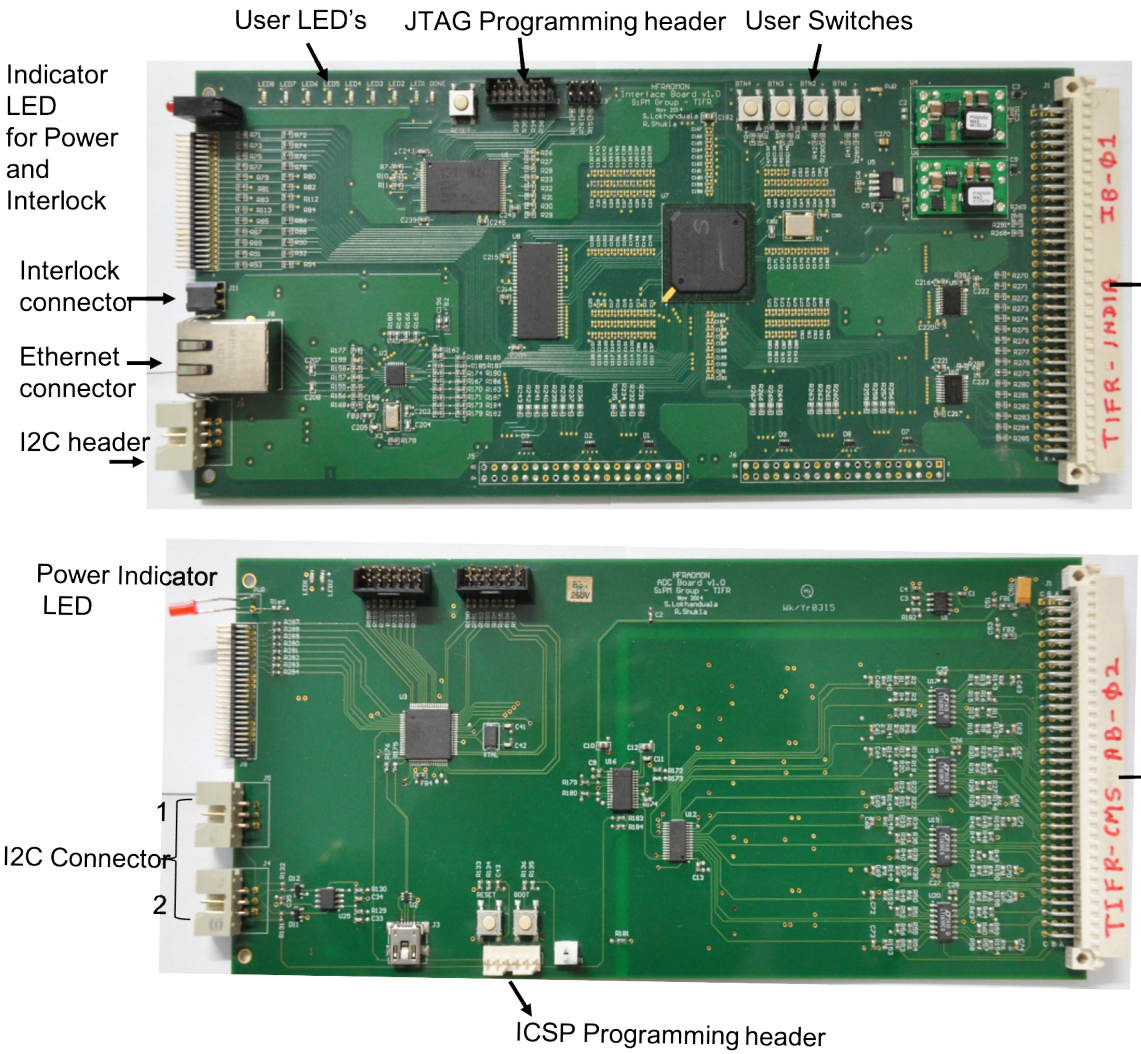
- **Control and Monitoring of 16 channels (detectors):**
  - **Control ON/OFF signaling (TTL)**
  - **32-bit count of asynchronous pulses (TTL), rate 1MHz**
  - **Voltage and Current Monitoring (Range: 0-10V)**
- **Readout: 10 Hz with Ethernet**

Block Diagram of the HFRADMON DAQ



Multiple ADC boards can be connected

- Both Boards comply to 3U standards



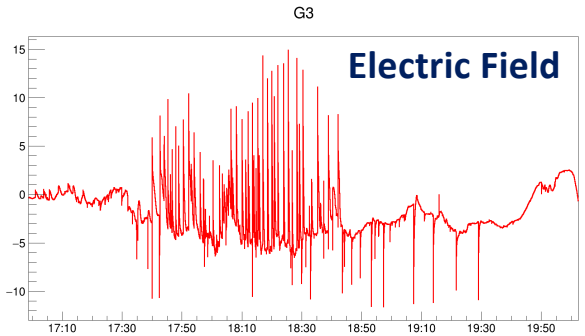
- **The hardware has been successfully installed and commissioned at P5 at CERN**
- **No issues reported**
- **Data is recorded online for debugging and monitoring purpose**

Trigger-less Muon DAQ (TM-DAQ) system for GRAPES-3 Muon Detector

Triggerless Muon DAQ Concepts and Physics Horizon

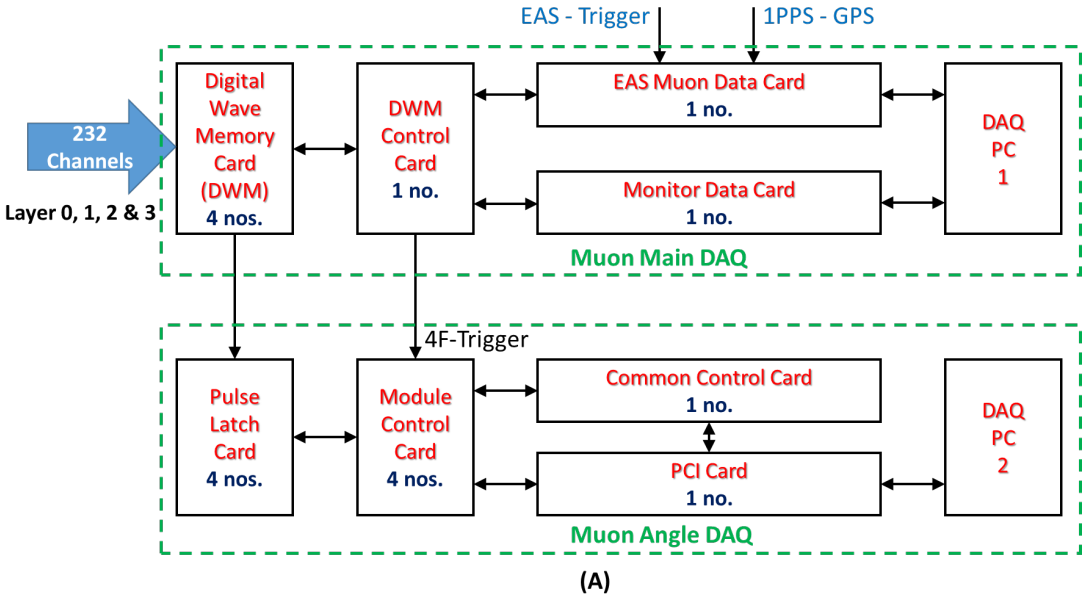
- **What is Triggerless Muon Data?**
  - **Record each and every hit due in proportion counter (Time and Pulse Width)**
  - **Record the hit rate of PRC, various triggers, temperature etc.**
    - **Pulse Width with a resolution of 10 nano-second**
    - **Absolute pulse arrival time with a resolution of 10 nano-second**
- **Do physics dependent reconstruction of raw data in offline mode**
  - **Rigidity dependent study of Moon Shadow**
  - **Transient Phenomenon**
    - **Thunderstorm Physics**
    - **Solar Physics**

    } **Better time resolution, muon multiplicity**
  - **Air Shower Physics**
    - **Air showers at large zenith angles, muon rich showers, Cosmic Muon Puzzle**
  - **New Physics**
    - **Search for tachyons, low beta particles (monopoles, WIMP etc.), serendipitous searches**



Existing DAQ Streams for Muon Detector

Existing DAQ
Two DAQ streams: Mu-Main and Mu-Angle
Mu-Main: Width and Time of each PRC w.r.t. Air shower trigger
Mu-Angle: Trigger rates in 15x15 angular bin histograms are recorded for 10 seconds interval
10+ large area PCB boards per modules
Large Deadtime: 12 – 20 %
Td resolution: 167 ns (Relative)
Arrival Time: Not measured
Width resolution: 333 ns
PWA spectrum measured for 1 channel (1000 sec) at a time in each layer time
No direct PRC's CRM 4F and Any3F at each second Other folds – time multiplexed
Zenith Angle measured up to Up to 45°



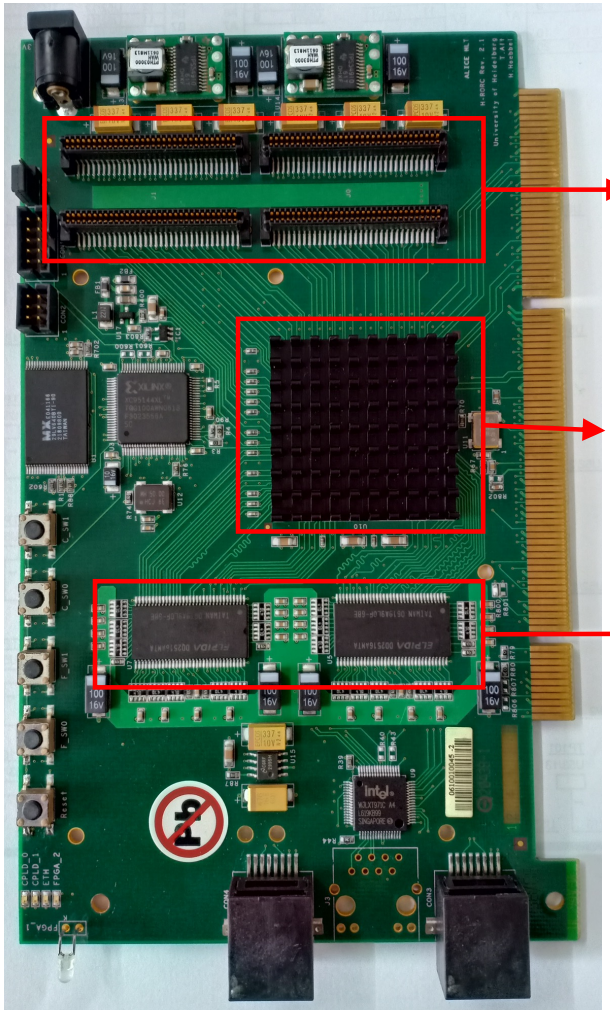
(A)

- **~10 Hardware power intensive cards per module designed in 20th century still working but difficult to maintain !**
- **Limited physics scope**

H-RORC (ALICE Board)

High-Level-Trigger (HLT) Read-Out Receiver Card (H-RORC) was used at LHC Point 2, CERN, Geneva during Run I phase of LHC

- System Requirement
  - Adequate I/Os for digital output proportional counter
  - Timing resolution, Excellent DSP ability, Memory
- Xilinx Virtex-4 FPGA (XC4VLX40)
  - High performance logic application series
- Clocks: 100 MHz & 50 MHz
  - Can be scaled up / down inside FPGA
- DDR SDRAM (EDD2516A)
  - 4 Physical chips of 32 Mbytes each
- Tyco connector
  - 158 Usable I/O Pins
  - 2 Layers (118 PRCs) per board



TM-DAQ/TCT Team

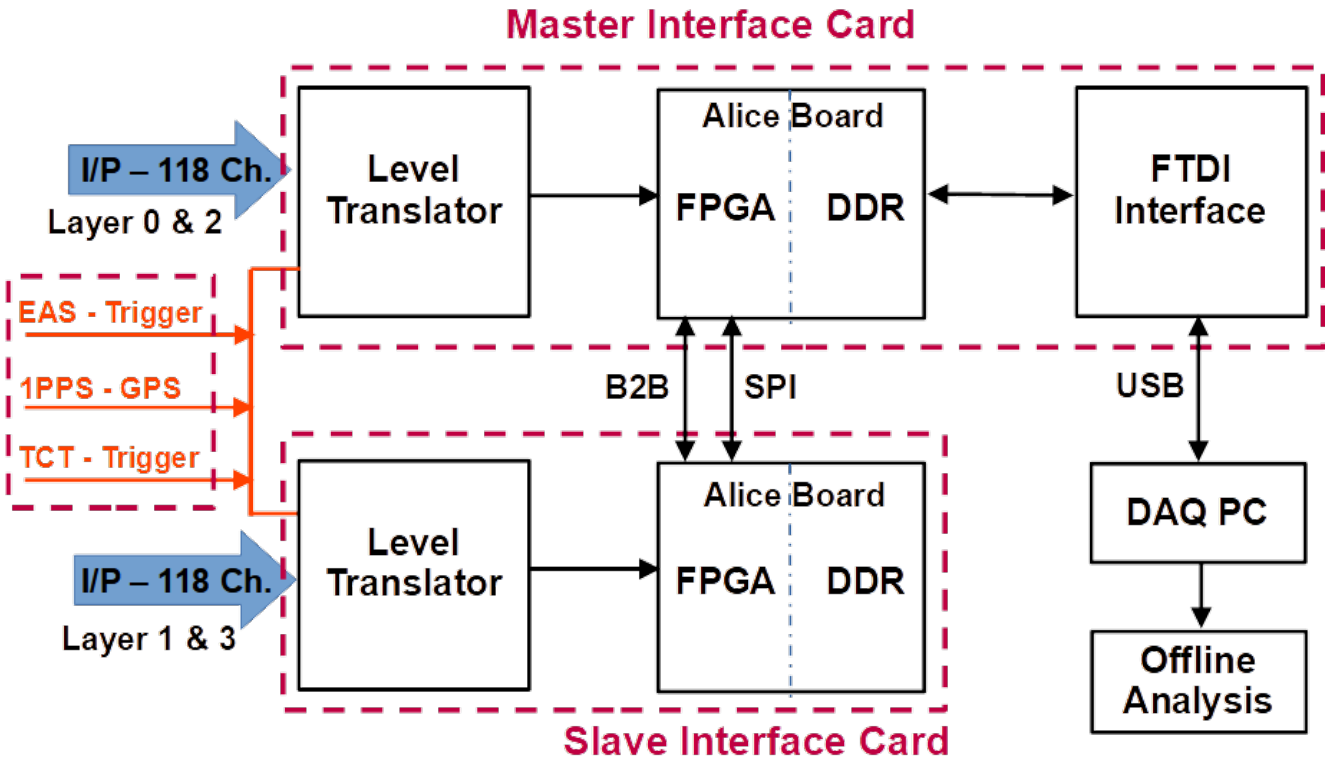
Hardware Tasks:

- Firmware Development and Integration for TM-DAQ System **(Pankaj Rakshee, RSK, AJ)**
- Design of Fabrication of Interface Card for TM-DAQ System **(K Manjunath, PR, RSK, AJ)**
- Time Calibration Trigger System for GRAPES-3 Experiment **(Atul Jain, PR, RSK)**
- Communication Protocols Used in TM-DAQ System **(R Suresh Kumar, PR, AJ)**

Software Tasks:

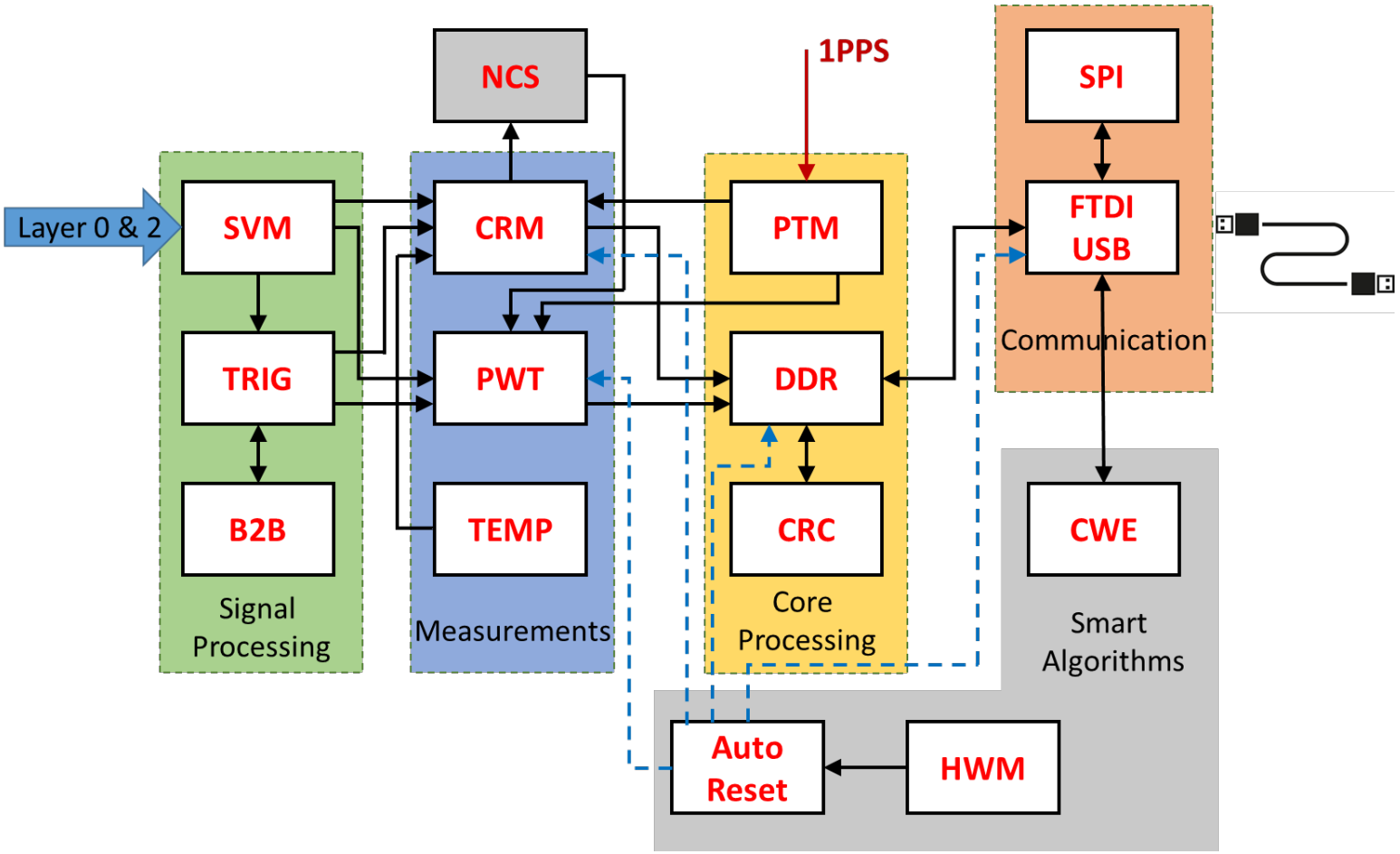
- Development of Software Framework for Monitoring, Analysis … **(Hari Haran)**
- Development of GUI for Data Quality Monitoring **(Siddiq Shareef, Hari Haran)**

System Block Diagram



EAS – Extensive Air Shower
PPS – Pulse Per Second
B2B – Board-to-Board
FTDI – Future Technology Devices International Ltd.
DDR – Dual Data Rate

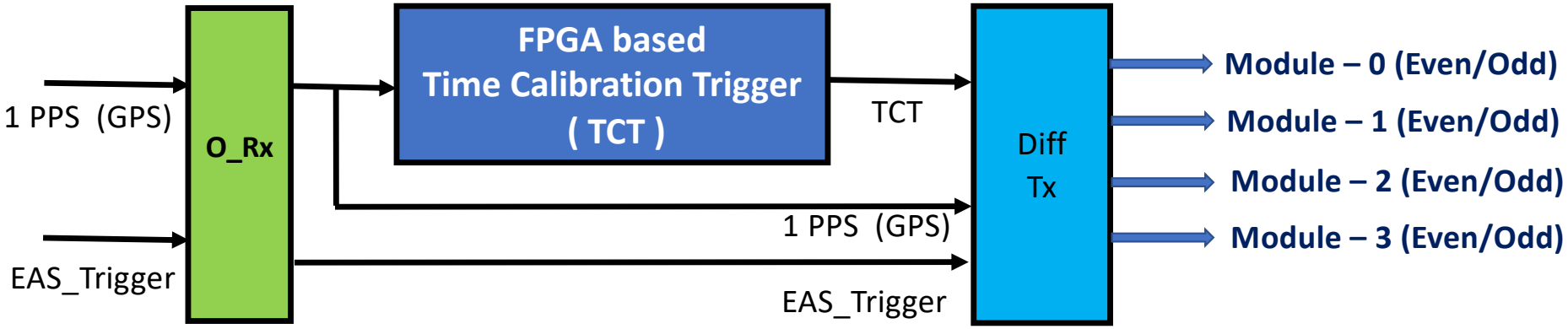
Block Diagram - Firmware



- B2B – Board to Board
- CRC – Cyclic Redundancy Check
- CRM – Count Rate Monitoring
- CWE – Control Word Exchange
- DDR – Dual Data Rate
- FTDI – Future Technology Devices International Ltd.
- HWM – Hardware Monitoring
- NCS – Noise Control System
- PTM – Precision Time Management
- PWT – Pulse width & Timing
- SPI – Serial Peripheral Interface
- SVM – Signal Validation Module
- TEMP – Temperature
- TRIG – Trigger
- USB – Universal Serial Bus

Time Calibration Trigger (TCT) System

- **GRAPES-3 Experiment has multiple Data Streams**
  - **Sc-Main, Sc-Rate, NaI, TM-DAQ (MuMain + MuAng), EFM**
- **Need a common timestamp for quick and reliable combined analysis**
- **TCT is FPGA based system that accomplishes this task**



Hardware Monitoring (HWM) and Auto Reset

Bit	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Des	DO	DI	SS	SCK	HW	DDR	DDR3	DDR2	DDR1	T3	T2	T1	TCT	EAS	FTDI	WR	RXF	TXE	PPS	INIT

B0 - INIT : After HW initialization and common for all checks

B1 - PPS : 3-5 pulses in 4 sec duration

B2, B3, B4 - TXE, RXF & WR : Some activity within 1 sec

B5 - FTDI : ANDing of TXE, RXF & WR

B6 - EAS : 15 – 80 counts in 1 sec

B7 - TCT : 9 – 11 pulses in 1 sec

B8, B9, B10 - T1, T2 & T3 : 5°C - 60°C

B11, B12, B13 - DDR1, DDR2 & DDR3: init_flag, err_flag etc. from DDR controller

B14 - DDR : ANDing of DDR1, DDR2 & DDR3

B15 - HW : ANDing of FTDI & PPS

B16 - SCK : (SPI Serial Clock) Activity within 2 sec

B17 - SS : (SPI Slave Select) Activity within 2 sec

B18 - DI: (SPI Data in) Activity within 2 sec

B19 - DO: (SPI Data out) Activity within 2 sec

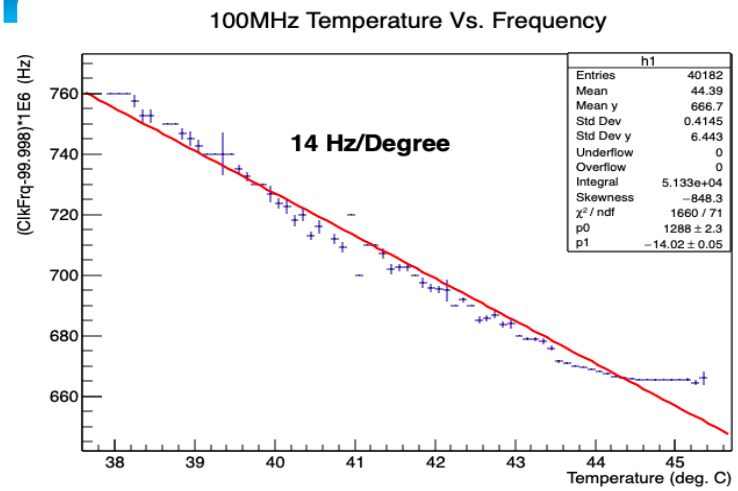
Auto Reset System:

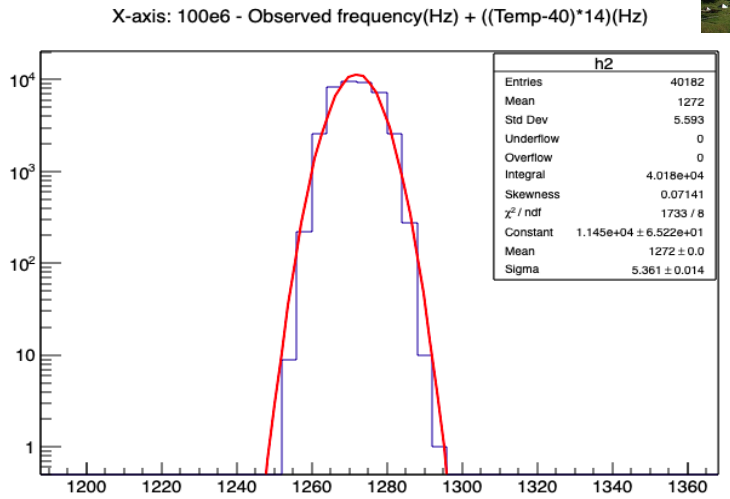
- An intelligent action taken by both FPGA and computer after sensing critical problem and DAQ run is resumed automatically
- Continuous hardware, FPGA firmware status, DAQ-computer software and data monitoring

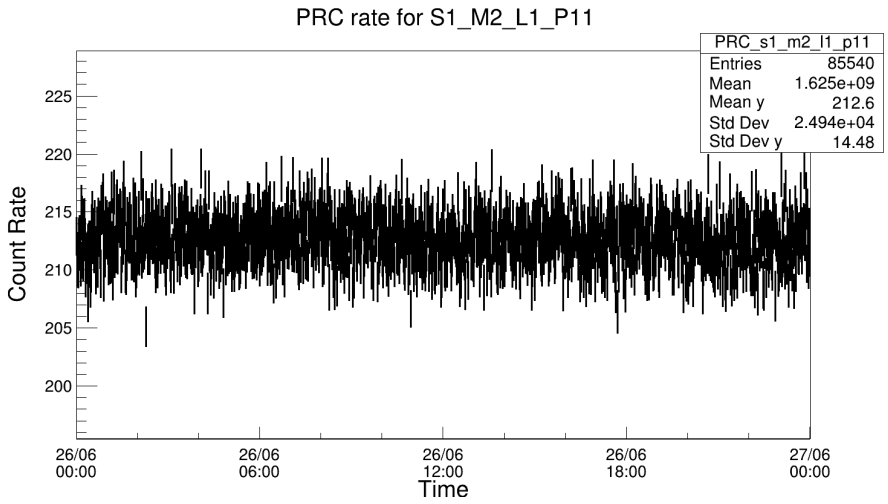
Comparison

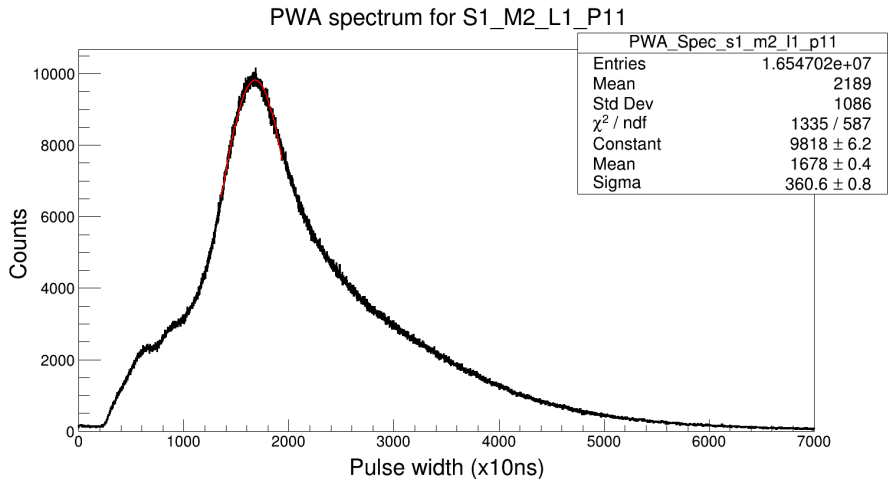
Sr. No.	Parameter	Existing DAQ	TM-DAQ
1	Systems	2 systems (Mu-main & Mu-angle)	1 System
2	Hardware	10+ Boards	2 boards
3	Dead Time	12 – 20 %	Very small (< 0.1%)
4	Td resolution	167 ns	Not applicable
5	Arrival Time	Not measured	10 ns
6	Width resolution	333 ns	10 ns
7	PWA	1 channel for 1000 sec in each layer time multiplexed	All PRC's, 4F, Any3F, EAS, TCT
8	CRM	• No direct PRC's CRM • 4F and Any3F at each second • Other folds – time multiplexed (1 in 14 at a time)	• All PRC's • All fold signals (4F, Any3F, 3F, 2F) • Layer OR signals • Box OR signals
9	Mu-Angle	Histogram of 10s packets	Each hit with arrival time (10ns)
10	Zenith Angle	Up to 45°	Up to 90°

Data Quality Monitoring

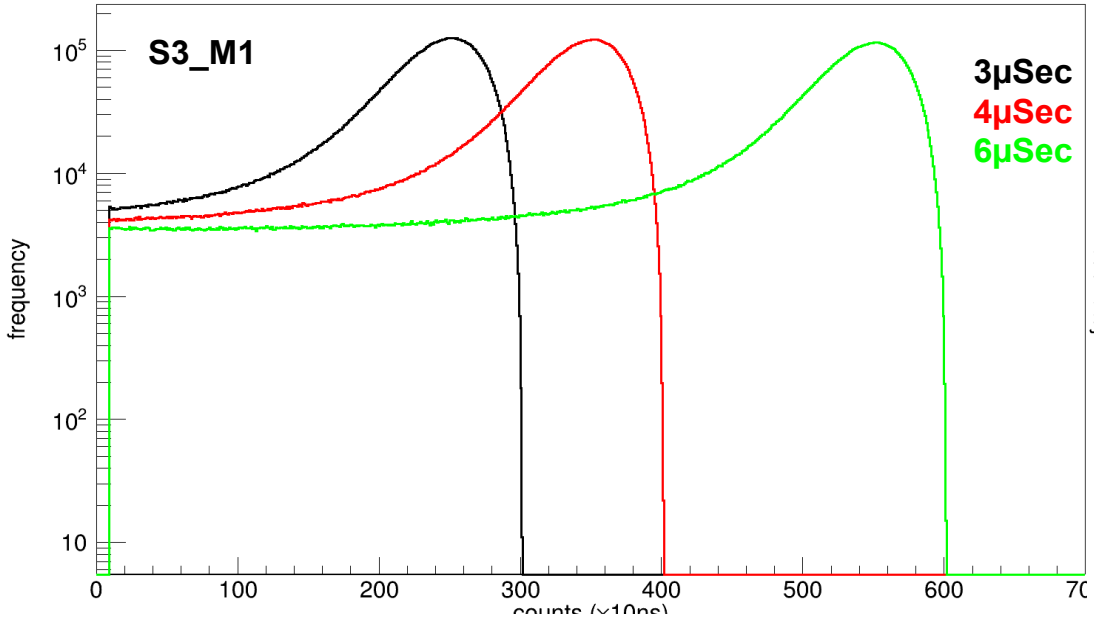


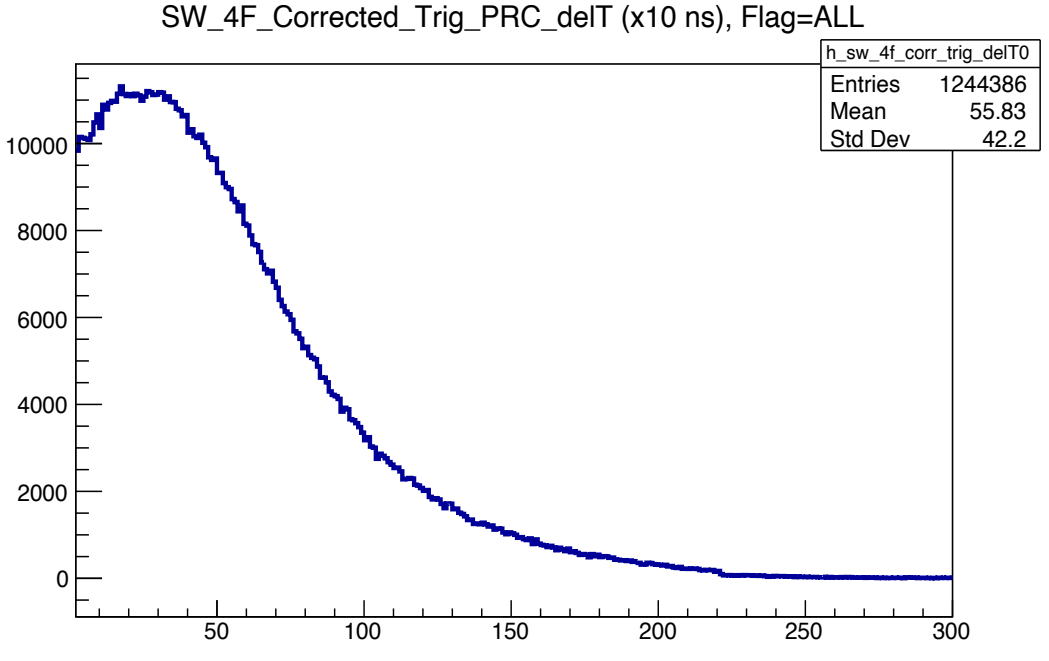






Study of trigger window

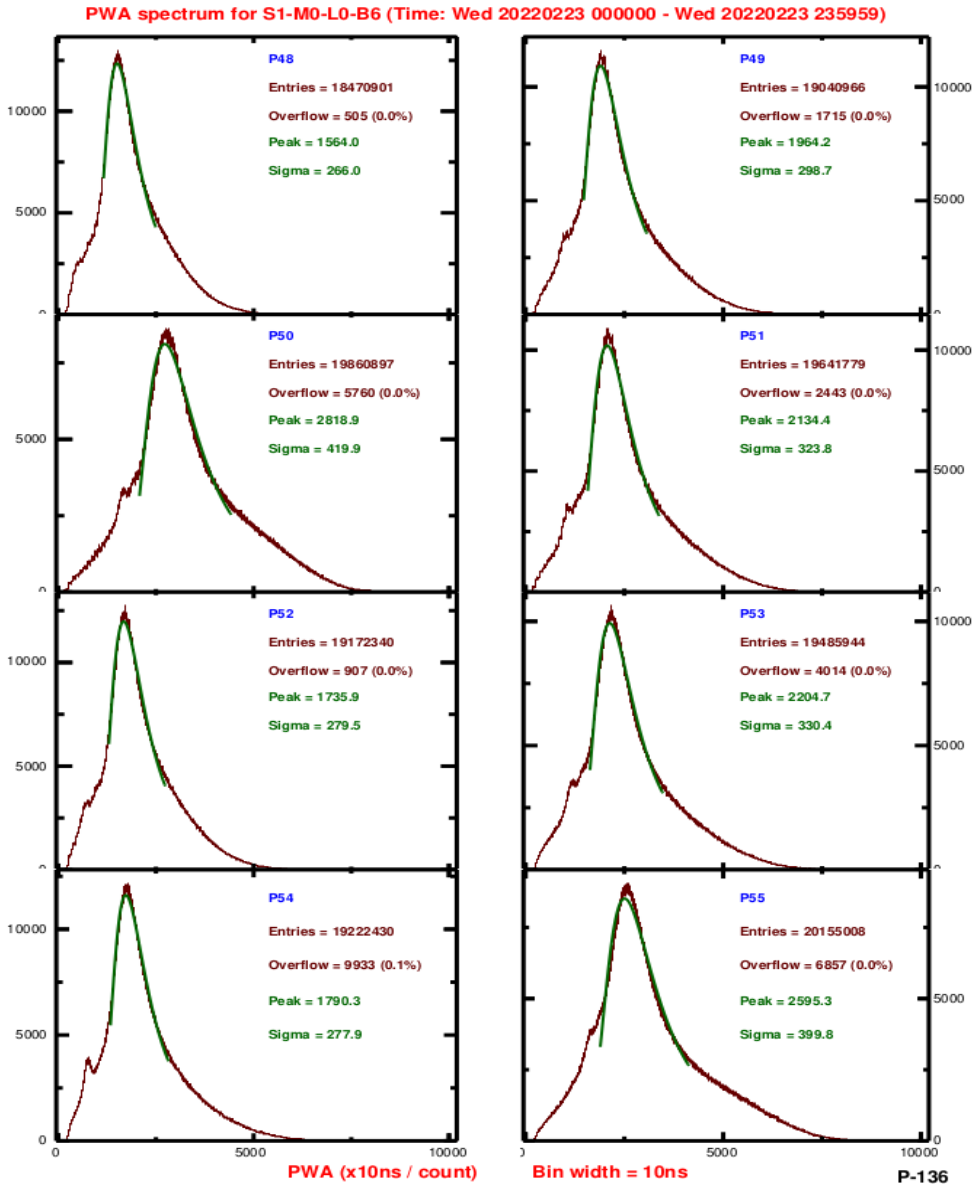




Tail on left side is mostly due to random hit forming HW 4F trigger

Hit Pattern A: X X X X **Hit Pattern B: X X X X X**

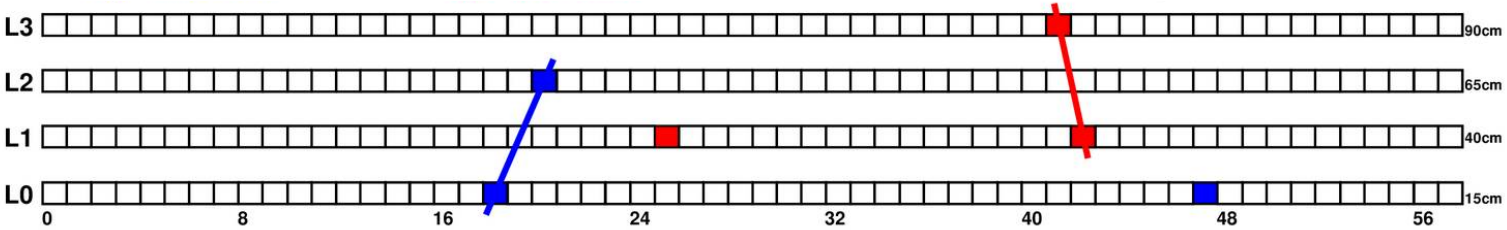
PWA Spectrum



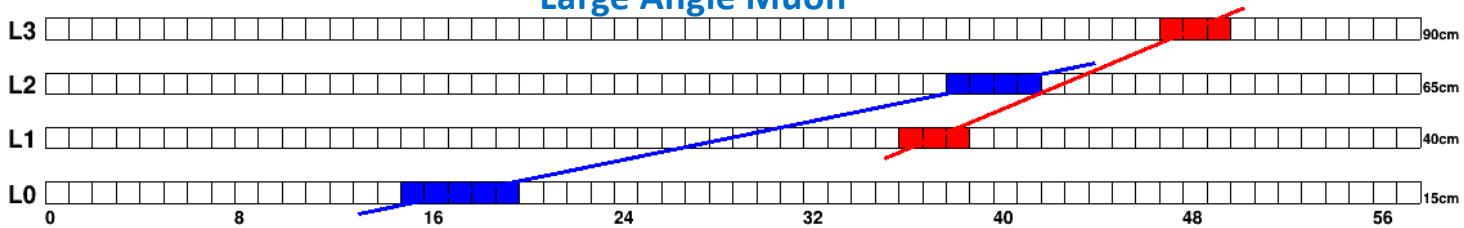
Software Framework

- ✓ Raw Data in Binary Format
- ✓ Raw Data in ROOT Format
  - ✓ Data Quality Monitoring
  - ✓ Shift Summary Plots
  - ✓ Graphical User Interface for Event Display
  - ✓ Reconstruction of Muons
- Physics Analysis … to begin after data validation

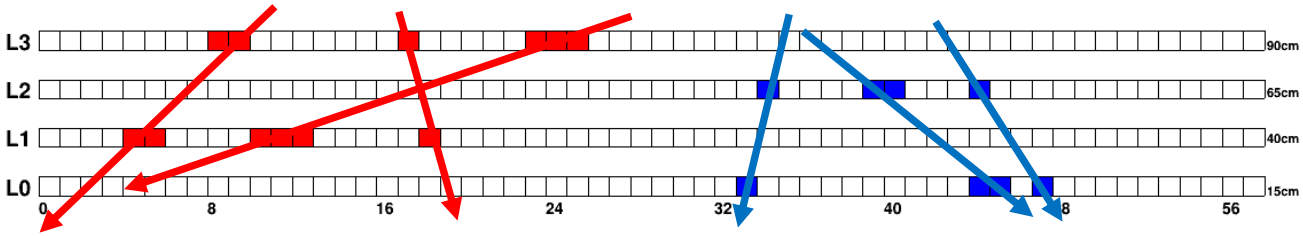
Single Muon

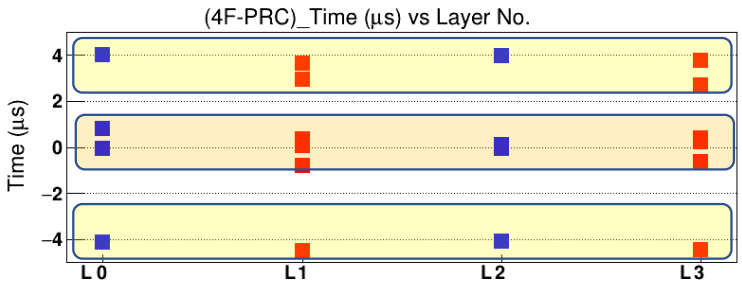


Large Angle Muon



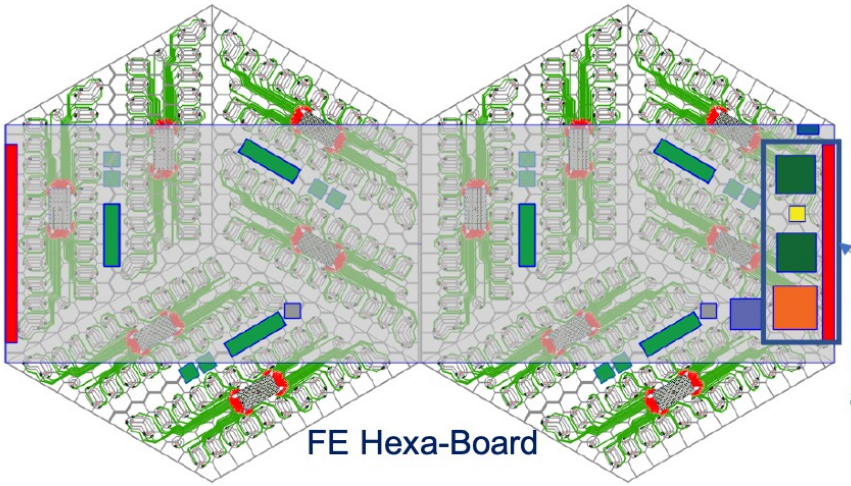
Three Uncorrelated Muon





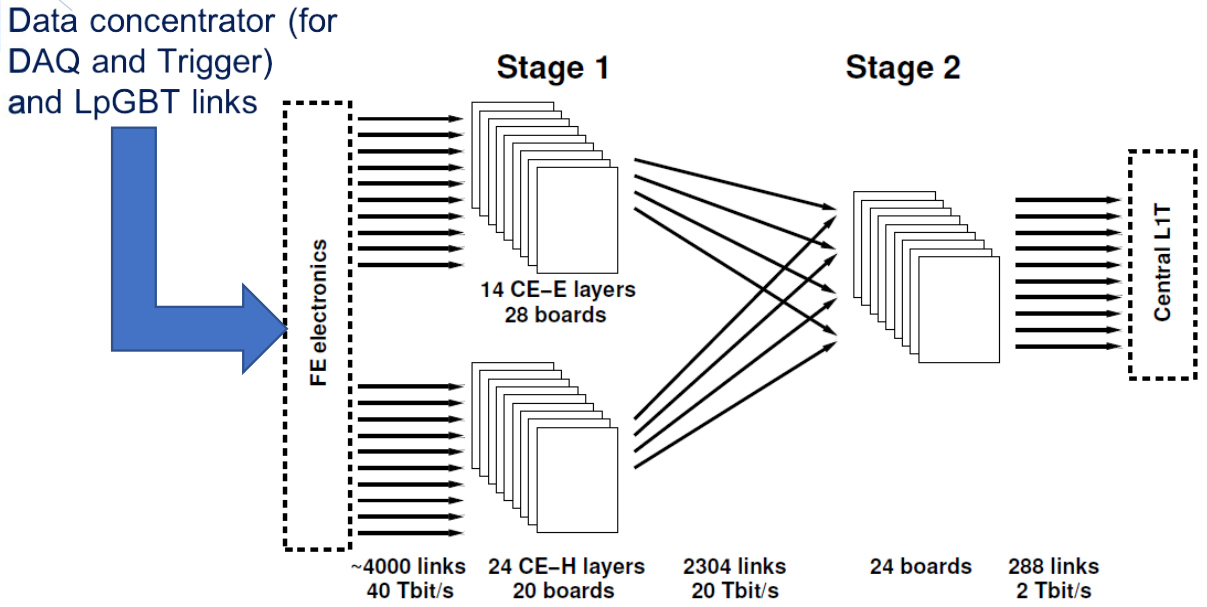
HGCAL: Trigger Primitive Generation System

HGCAL Data Flow: Front-End To Backend



On Detector

- TPG board will have 96 I/O optical links
- Xilinx VU9P Ultra-scale + FPGA chosen for the job
  - 104 high speed transceiver capable of 25/16 Gbps.
  - As of now 16 Gbps maximum to be used



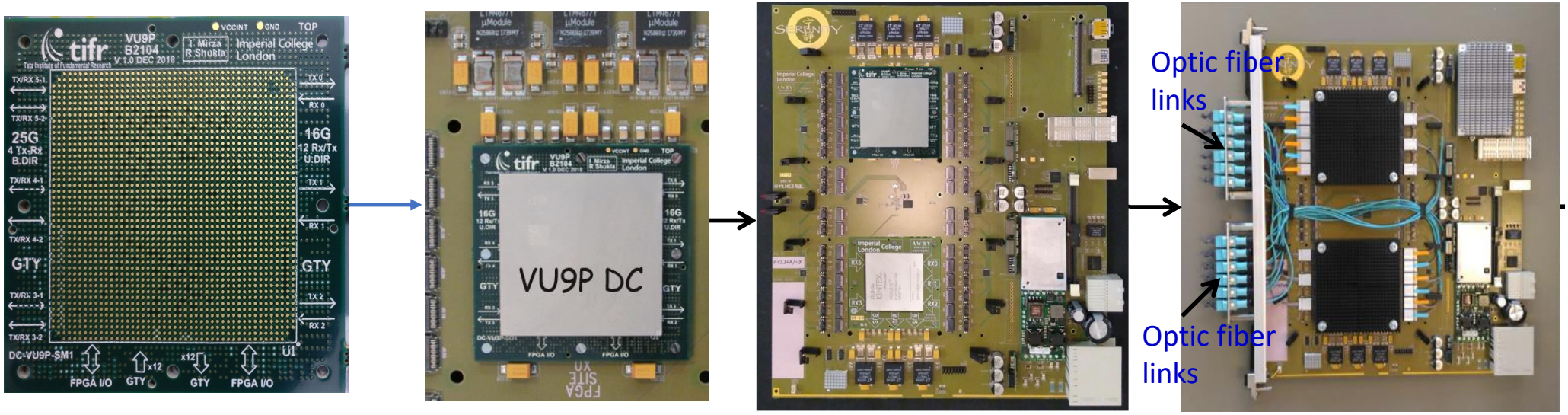
In counting room

Trigger Primitive Generator (TPG) board

- Raw data coming from selective sensors on LpGBT links
  - Only the first and subsequent alternate layers from the CE-E, i.e. 14 of the first 28 layers.
  - All 24 of the CE-H layers.
- Different types of raw data
  - 2x2 sum and 3x3 sum
  - Sum all channels read by HGROC (energy map)
  - Zero suppressed at FE, thus different latency (size) at each BX
- Maximum latency (set by FE concentrator) to 12 BX: 300 ns
- Two stage system (identical hardware)
  - Trigger primitives passed on to central L1 correlator to take L1 decision (within 5 us)
  - VU9P FPGA daughter card on common hardware board
- TIFR has successfully completed two major responsibilities:
  - Development of PCIe framework: HDL framework for FPGA, driver and software for PC. Integrated into standard uHAL framework and subsequently algorithm development framework
  - Design and Fabrication of Xilinx Virtex Ultrascale Plus FPGA (VU9P) Daughter Card (DC)

Manufacturing of Serenity and Daughter cards in India

- Collaborated with Micropack, Hyderabad
- Careful layer stack re-design (16L) as per Micropack capability and available materials without compromising specifications of the design
- Two daughter card versions and Serenity successfully fabricated in India!
- Extensive QC being carried out at TIFR before assembly
- Test stand with Serenity being setup at TIFR



Summary

- **Future of Digital Signal Processing is indeed embedded into the ES**
  - **Parallel Processing, Machine Learning, High Speed Communication etc.**

- **Engineering team of the DHEP is well poised to extract the best using ES as per the given application**
  - **Students should be trained and encouraged to participate in such activities of core importance**

Acknowledgement: Several slides adapted from presentations of:

Atul, Hari, Irfan, Manju, Pankaj, Raghu, Siddiq, Suresh

THANK YOU