Progress of G-APD (SiPM) based Imaging Camera for ACT

(S.S.Upadhya, on behalf of HAGAR group, TIFR, Mumbai)

- Introduction

- Camera specifications

- Challenges faced

- Design & Development (Front End & Back end)
    - *Status & Results*

Camera Specifications

- Imaging camera housed at focal point of 4m telescope

- Operational site is Hanle.
  - *Temp variation of 10^oC over a night and Avg night temp varies -20^oC to +20 ^oC over the year*
  - *Observation condition : Dark to Bright night sky regions or Twilight condition*

- 256 pixels Camera
  - *FOV 5^ox5^o (353x353mm)*
  - *Pixel Size 0.31^o (22.1x22.1mm)*
  - *Pixel Sensor S13361 : G-APD(SiPM) of 4x4 array (13x13mm), Sub-pixel of 3x3mm size*

- Detection of Cerenkov flashes (~5ns) of few 10s of pe against large NSB back ground(93Mpe/s per pixel)

- Pixel information to be recorded
  - *Pulse profile@1GSPS or Charge*
  - *Dynamic range up to 1000pe/pixel with a resolution of 0.5 pe (up to 10pe)*

- In-situ calibration of pixel gain of Camera and gain stability monitoring

- Trigger criteria: 4 near neighbor pixels crossing set pe threshold and rate is Few tens of Hz
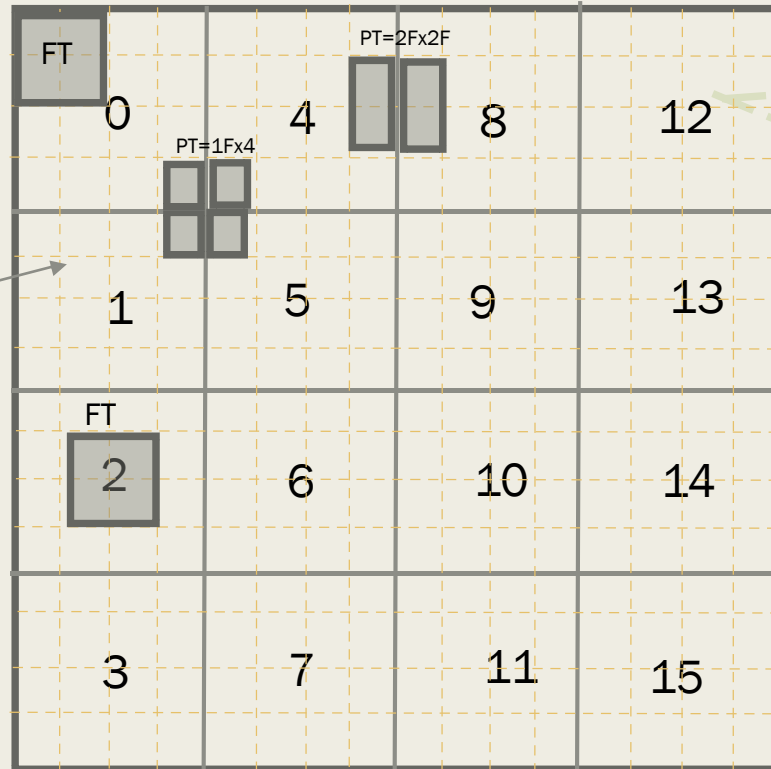
Challenges faced

- Due to limitation of light concentrator, sensor area could not be optimized less than 12mm^2 and 4x4 array SiPM used. Due to large decay of SiPM pulses, individual 16 sub pixel pulses are processed & added in electronics for better S/N ratio

- The detection of faint Cerenkov photon shower of 10s of photons in few nano-seconds window against continuous huge night sky photons of 93Mpe per second per pixel during dark night observation, which increases further in observations under bright sky region or moon lit condition.

- The physics need of wide dynamic range from single photon to 1000 photons per pixel.

- Extreme night temperature of +30°C to -25°C in the site Hanle(4300m Altitude), Ladakh where the Camera is planned to be deployed. SiPM gain is sensitive to temperature and hence Bias voltage is need to be compensated continuously by monitoring temperature near SiPM (G-APD)

- Space constraints of front end electronics (< 22.1mm width PCB needs to accommodate 16 subpixel fast analog signal conditioning electronics) demands choice of SMD component design with 10 or more layers PCB. This miniaturization makes PCB population (soldering) very challenging during in-house prototype development.

- High data through-put due to Giga sampling of the pulse profile

- In-situ gain calibration and monitoring

- Due to space constraint and complexity of the design, FPGA and microcontroller are chosen. This demanded self up-gradation of staff skill to these new technological designs from the conventional discrete logic design.
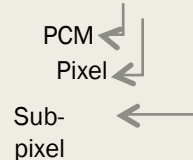
Pixel view of Camera(256 pixels)
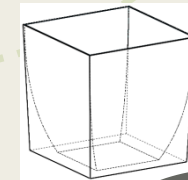

Camera (16 Clusters)

Trigger criteria
FT & PT

Cluster

A cluster of 16 pixels
Pixel size 22.1x22.1 mm
1..11
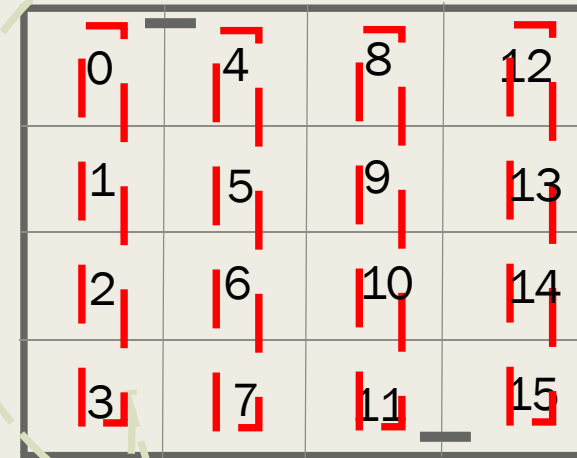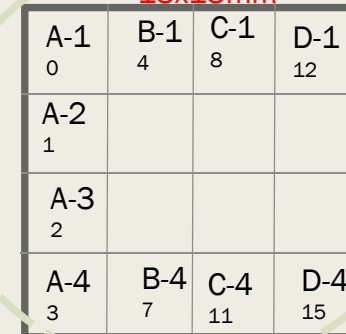
HV9 to 16, D,3.3V,Gnd
11...
1

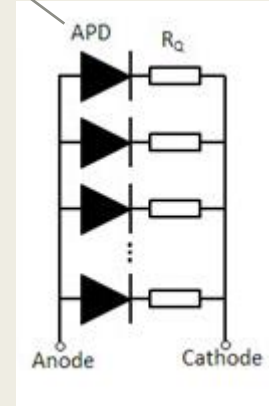Light concentrator
$22.1mm^2 >> 12.4mm^2$
L=24.5mm

Sub-pixel
3x3mm

Pixel ID :: XXxxxx hex

PCM
Pixel
Sub-pixel

• Sub-Pixel status in a Pixel
xxxx
A1..4, B1..4, C1..4,D1..4
(P0............7,   P0............7)
(LSB......................   MSB)

4X4 G-APD
13x13mm

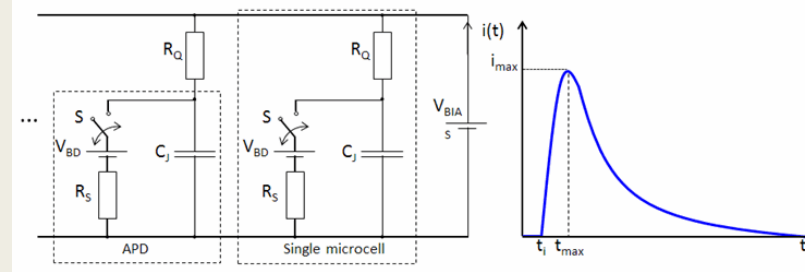| A-1 0	B-1 4	C-1 8	D-1 12
A-2 1			
A-3 2			
A-4 3	B-4 7	C-4 11	D-4 15
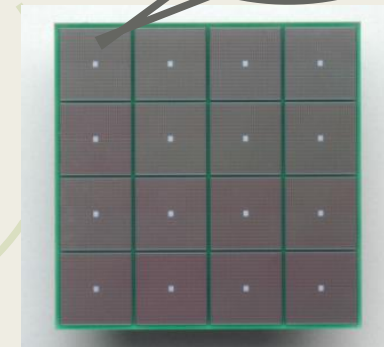
Hammatsu **S13361-3050AS-04**

Pixel Sensor: 4x4 GAPD (Hamamatsu S13361-3050AS-04)

13x13mm – 4x4 array, <u>74% Fill Factor</u>

Sub pixel Specifications

- Sub-pixel : 3584 micro-cells of 50 μm pitch
- Low voltage (Vop=56V Typ.) operation
- High gain: 10^5 to 10^6
- Operating temp -20 to +60C
- Spectral Response 270 to 900nm Peak at 450
- PDE 40% at 450nm
- <u>Dark count per Sub pixel typ 0.5M Hz at 25C</u>
- <u>Cross talk 3%</u>
- <u>Temp coeff of BD voltage is 52mV/C</u>
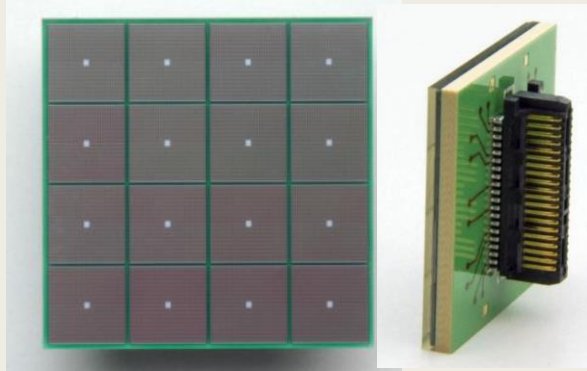
Characteristics Vover dependence (measurement example)
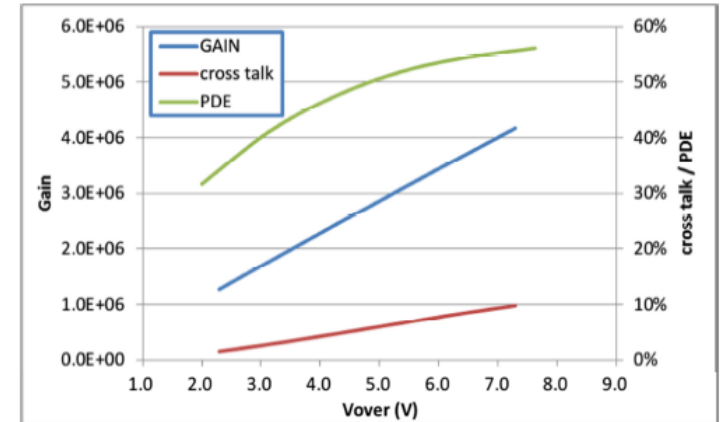
Photon detection efficiency vs. wavelength (measurement example)

Pixel 4x4 array (OV=Vbias- Vbr)

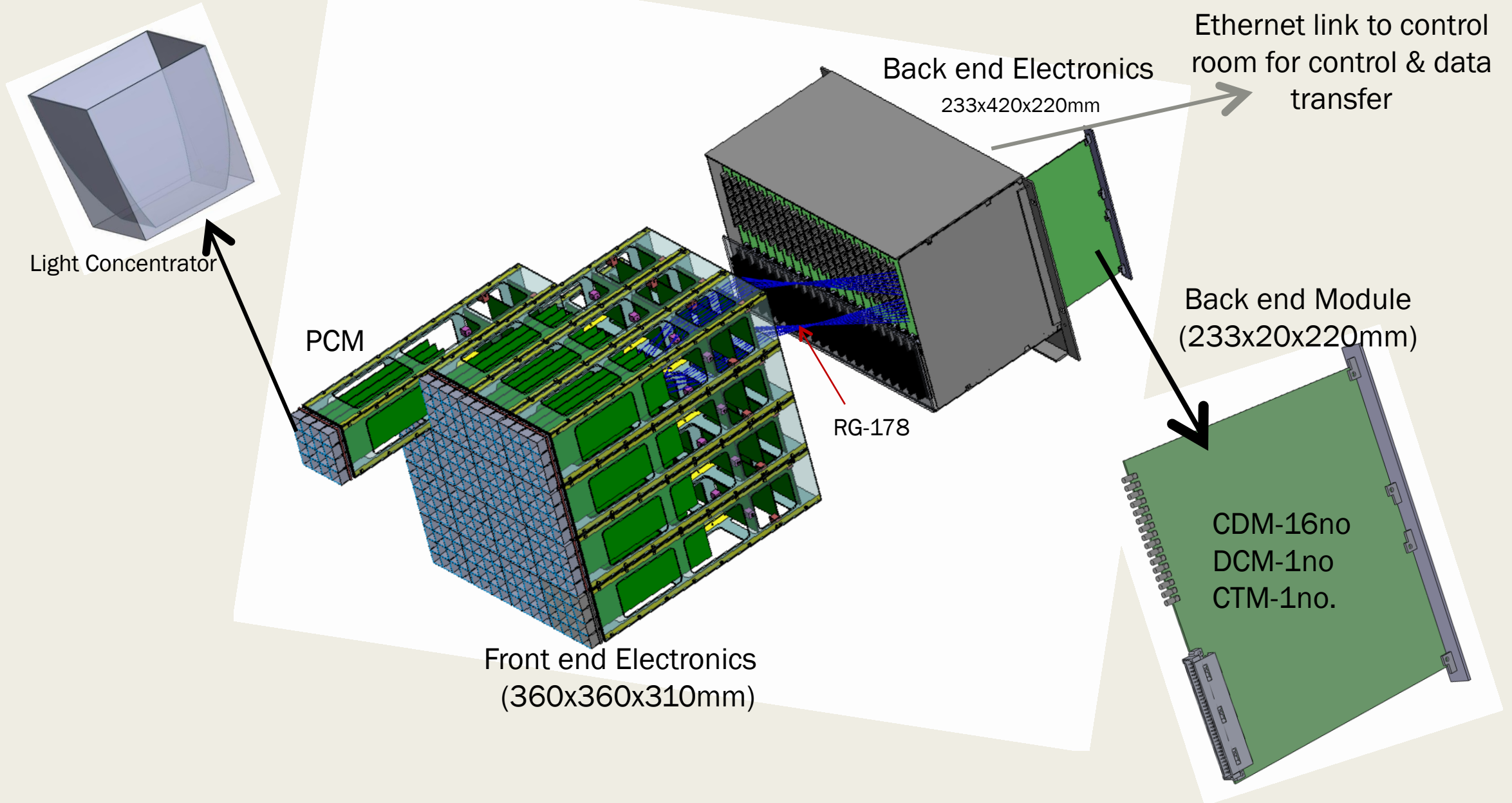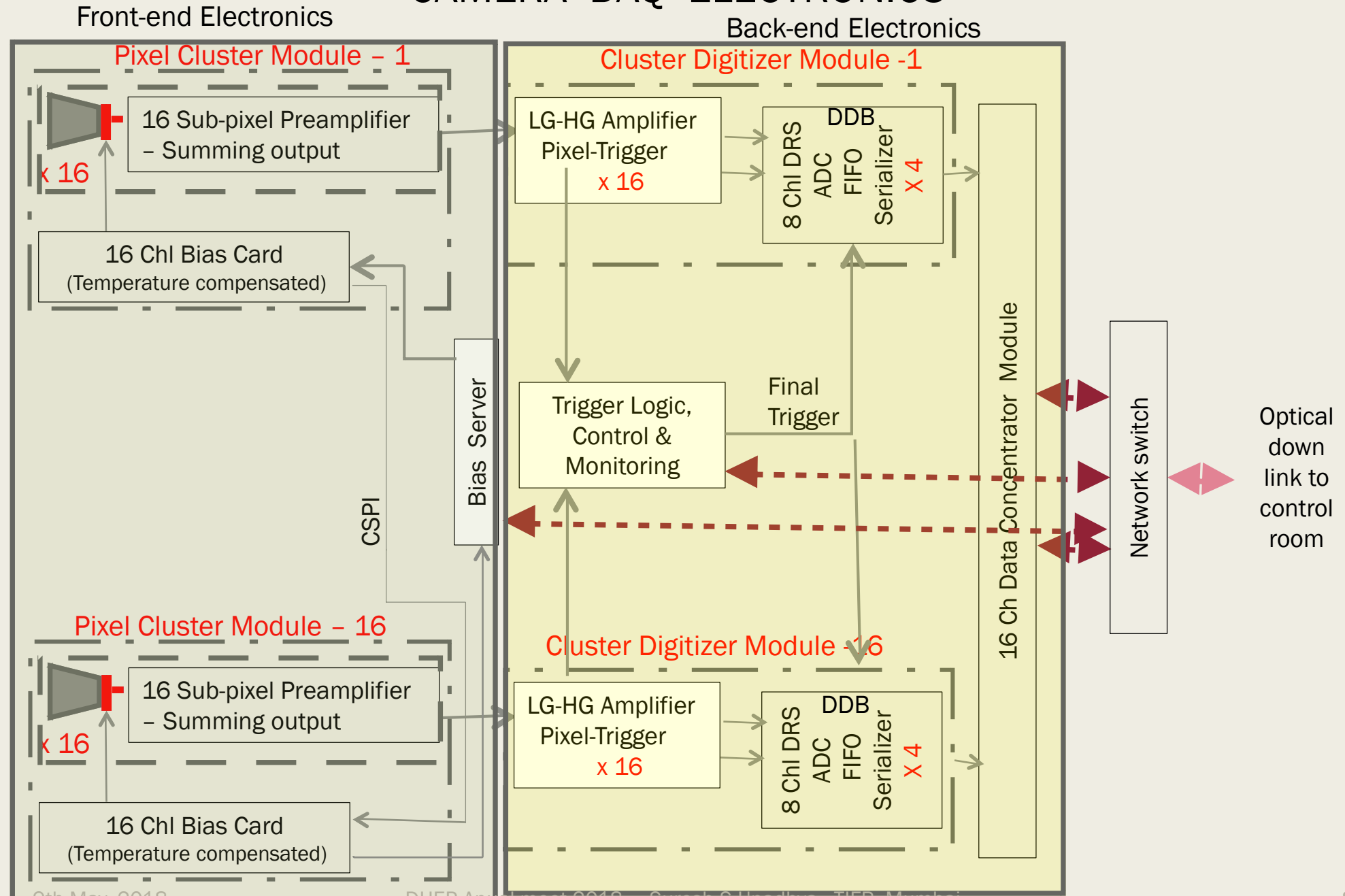- <u>Common Bias</u> : Gain variation of 1.25% @ 3V OV
- <u>Gain variation</u> of 1.5% per C
- <u>Dark counts</u> of 0.5 x16 = 8MHz, temperature dependant

Imaging Camera Electronics in focal plane of telescope

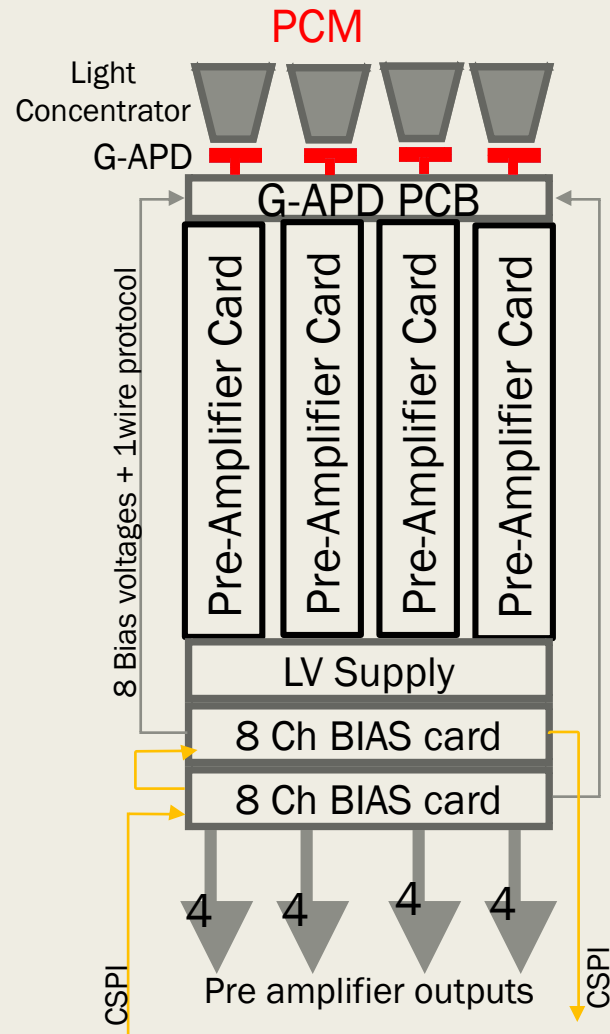Light Concentrator

PCM

Front end Electronics
(360x360x310mm)

RG-178

Back end Electronics
233x420x220mm

Ethernet link to control room for control & data transfer

Back end Module
(233x20x220mm)

CDM-16no
DCM-1no
CTM-1no.

CAMERA DAQ ELECTRONICS

Front-end Electronics

Back-end Electronics

Pixel Cluster Module – 1

16 Sub-pixel Preamplifier – Summing output

x 16

16 Chl Bias Card
(Temperature compensated)

Cluster Digitizer Module -1

LG-HG Amplifier
Pixel-Trigger
x 16

DDB
8 Chl DRS ADC FIFO Serializer X 4

Trigger Logic, Control & Monitoring

Final Trigger

Bias Server

CSPI

Pixel Cluster Module – 16

16 Sub-pixel Preamplifier – Summing output

x 16

16 Chl Bias Card
(Temperature compensated)

Cluster Digitizer Module -16

LG-HG Amplifier
Pixel-Trigger
x 16

DDB
8 Chl DRS ADC FIFO Serializer X 4

16 Ch Data Concentrator Module

Network switch

Optical down link to control room

Pixel Cluster Module Components

- **Pixels Cluster Module(PCM) -16no.s**
  - *Hollow Light concentrator- 16 no.s*
    - Square Entry(22.1mm) & Exit(12.4mm), H=25.5mm
    - Concentrates pixel light onto G-APD
  - *GAPD PCB – 1no.*
    - Houses 16 pluggable G-APDs (4x4 sub pixels)
    - Two temperature sensors
  - *Pre-Amplifier Card – 4no.s*
    - Has 4 Pixel channels. Each Channel processes16 sub-pixel signals
    - 16 sub pixel pulses are amplified(Transimpedance), shaped and summed to get a pixel signal output
    - Each Sub pixel can be Enabled/Disabled in all 4 pixels using 1-wire protocol.
  - *Bias Card-2no.s*
    - 8 channel, 0 to 70V Bias voltage, 2.5/4mA
    - Micro-controller based control & monitoring
    - G-APD gain Compensated for Temperature & load variation
    - 1 wire connectivity to Temperature sensors and Sub pixel selection
    - CSPI link to Raspberry Pi based Bias server for overall control & monitoring of 32 Bias cards in 16 PCMs
    - Raspberry Pi has Ethernet down link to remote server in control room
  - *LV Supply*
    - Caters required voltages to all the cards in a PCM

Pixel Cluster Module

Pixel Cluster Module

14W
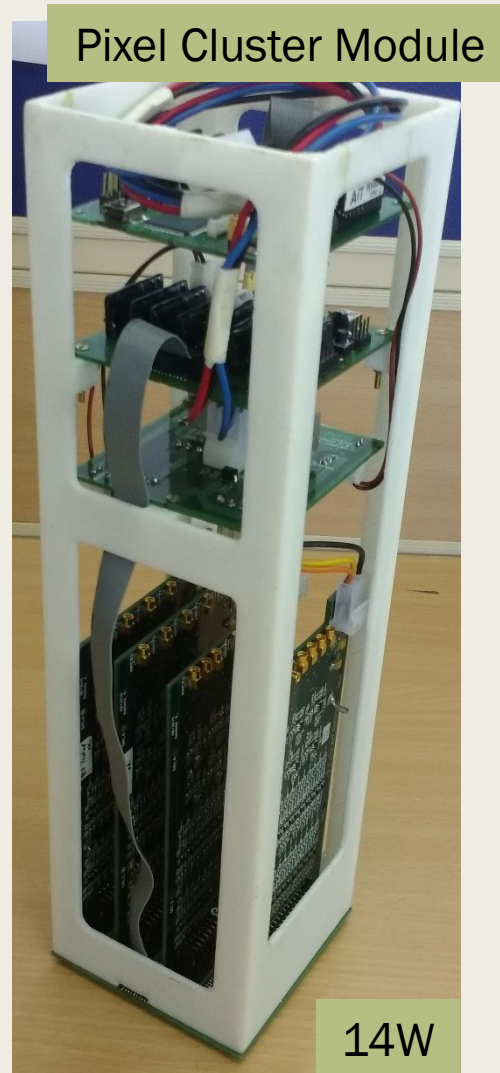
BIAS

Pixel GAPD Board
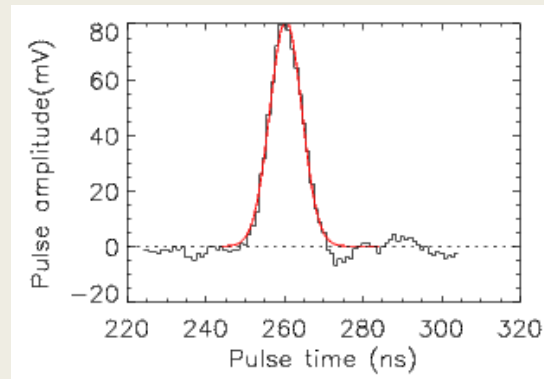
Amplifier with test ZIG & CDM
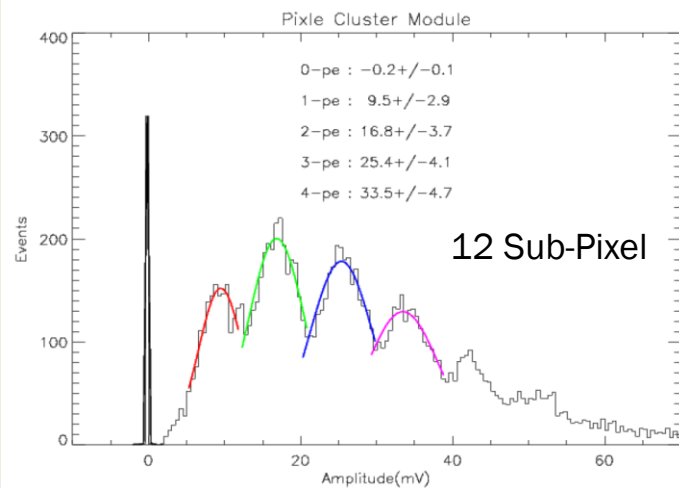
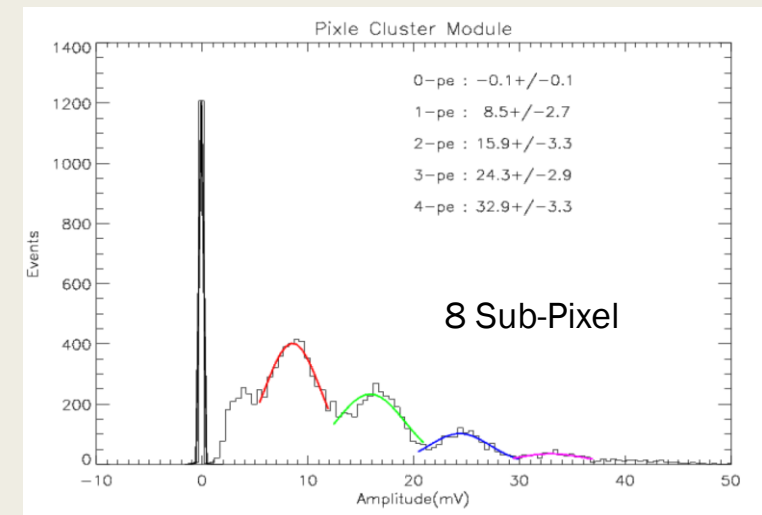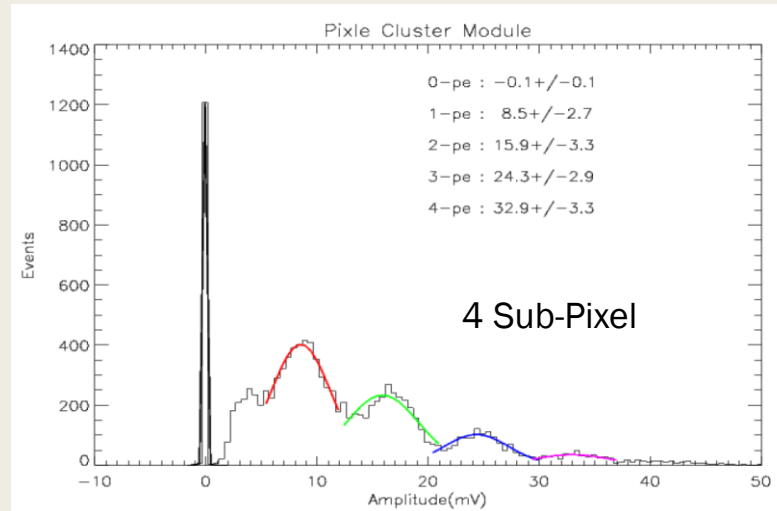LV supply board

4 Channel Amplifier

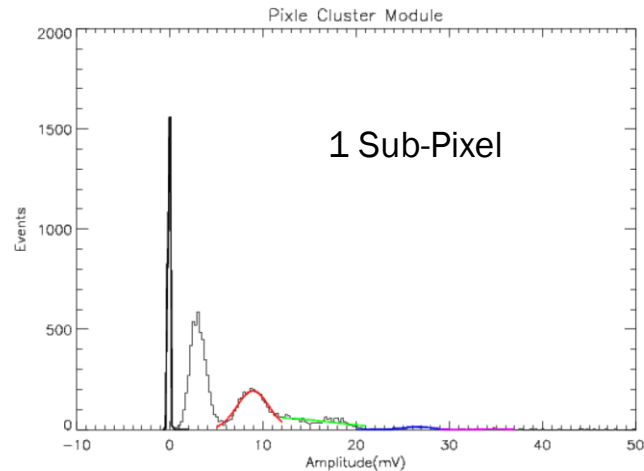Amplifier with test ZIG & CDM

- One PCM is ready for rigorous tests

# Pixel Amplifier PG test result (Version 2)

Linearity of GAPD Amplifier-1

$y = 55.738x + 6.9997$
$R^2 = 0.9997$

Peak output voltage, mV

Peak Input Current, mA (1 pe -> 15 µA @ OverVoltage = 3 V)

Summation of Sub-pixels using input jumpers

$y = 55.167x + 13.945$
$R^2 = 0.9997$

O/P in mV

Input in mA

- Series1

Summation of Sub-pixels using En/Dis

$y = 56.367x + 2.932$
$R^2 = 0.9999$

OutPut voltage, mV

Current, mA (1 pe -> 15 µA @ OverVoltage = 3V)
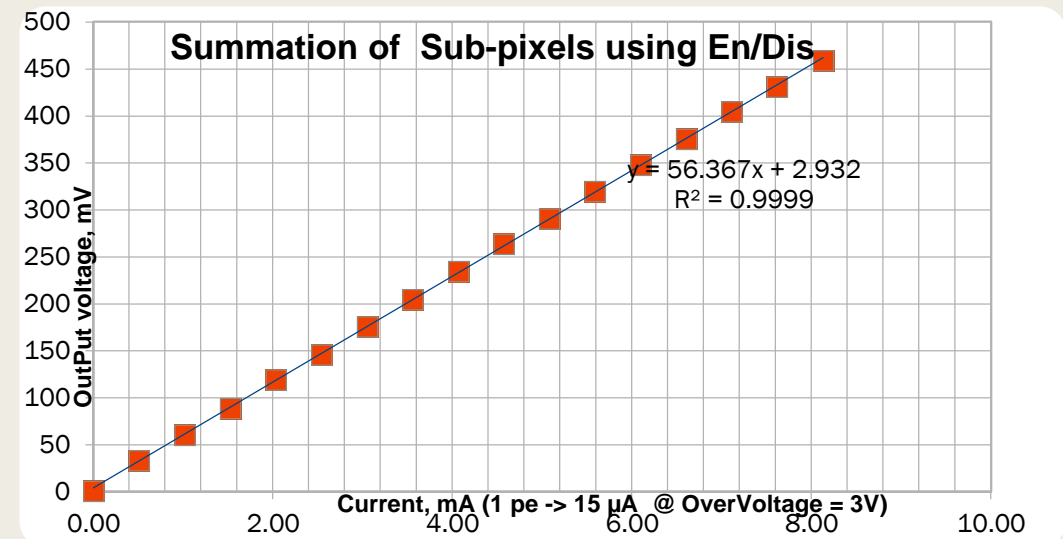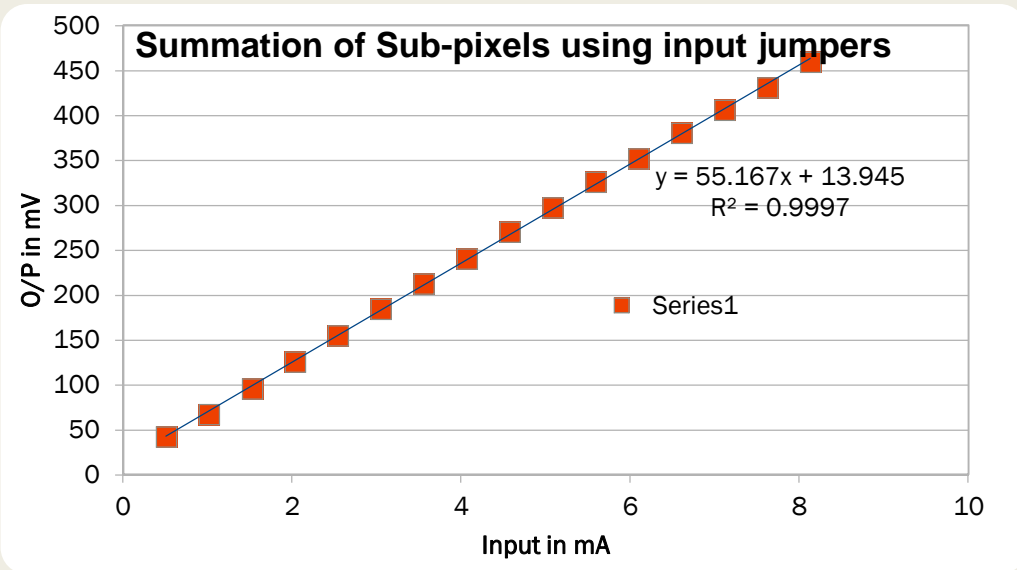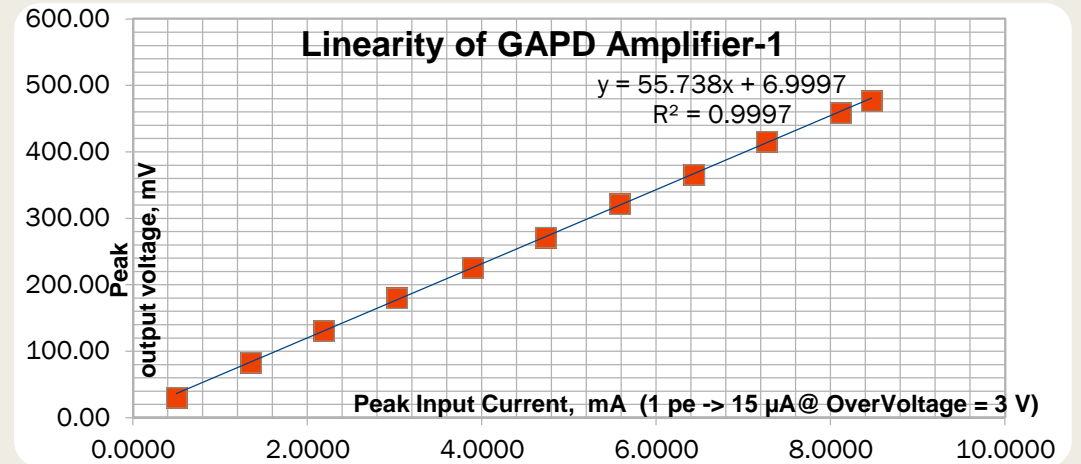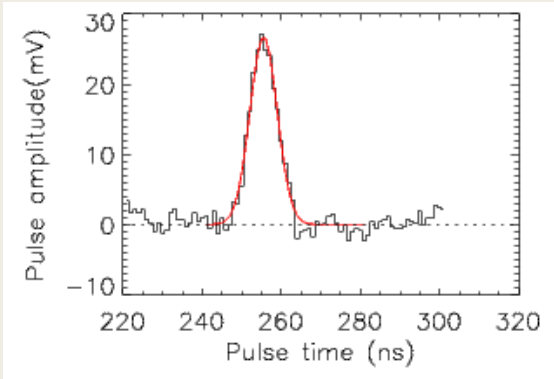
Summation results using GAPD exposed to __LED flasher__ (Amplitude spectrum)
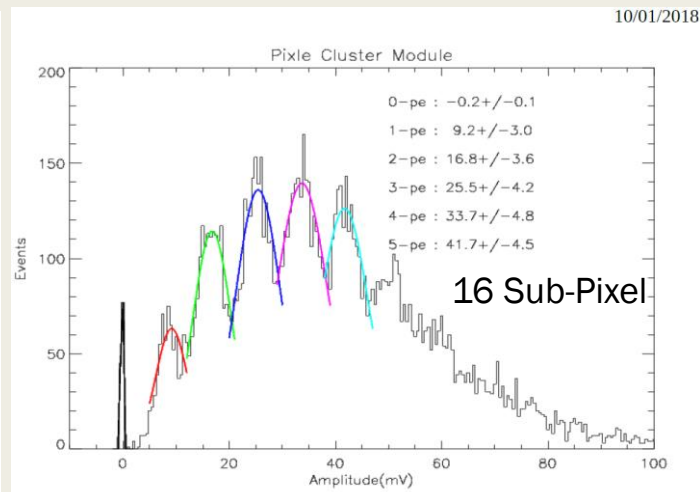
| N SubP	PtoP Amplitude					Average	StdDev
1	9						
4	8.6	7.4	8.4			8.133333	0.64291
8							
12	9.7	7.3	8.6	8.1	0	8	0.655744
16	9.4	7.6	8.7	8.2	8	8.125	0.550757
						8.13333	0.64291
					AVerg	8.086111	0.61647
					StDev	0.07469	0.05727

Summation results using GAPD with LED flasher (Charge)

1 Sub-Pixel

4 Sub-Pixel

8 Sub-Pixel

12 Sub-Pixel

16 Sub-Pixel
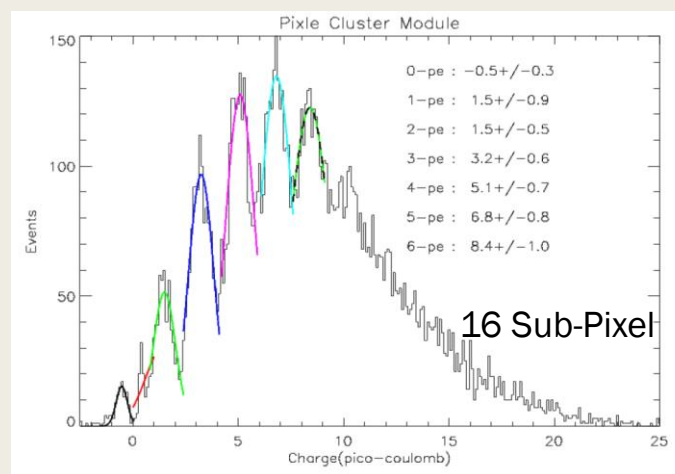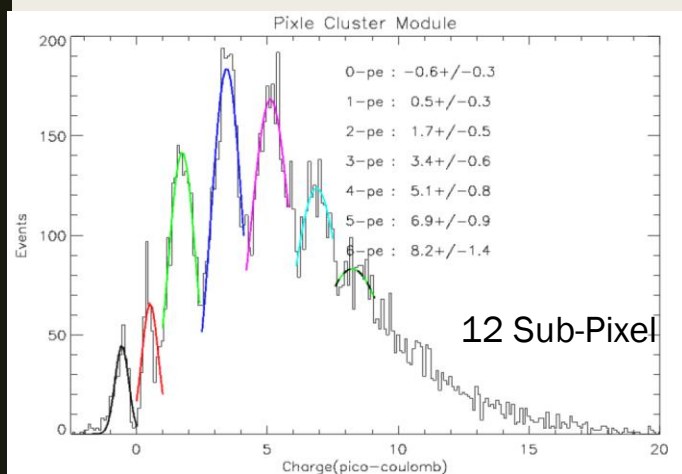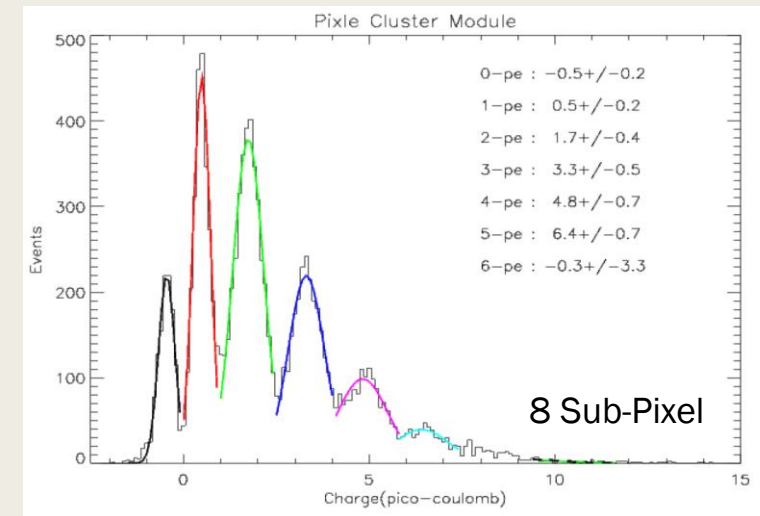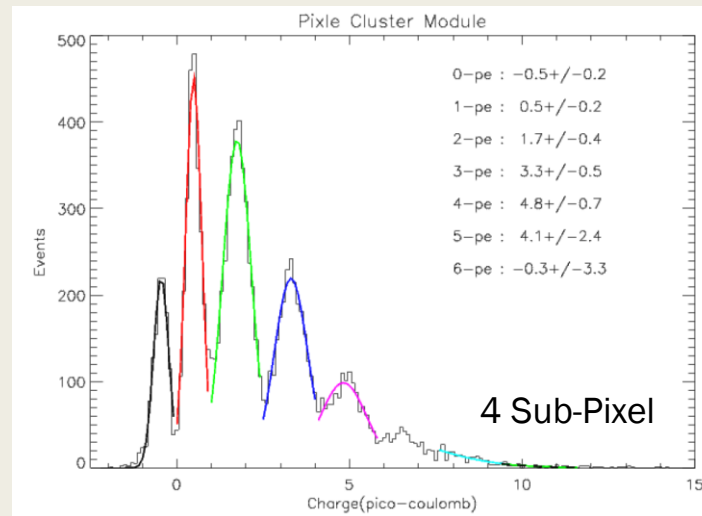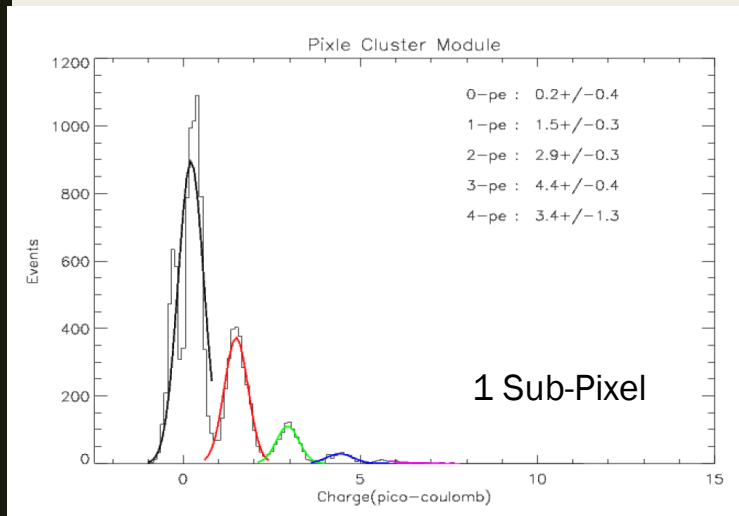
N SubP	PtoP Charge					AVerage	Std. Dev
1	1.3	1.4	1.5			1.45	0.1
4	1	1.2	1.6	1.5		1.433333	0.275379
8	1	1.2	1.6	1.5		1.433333	0.275379
12	1.1	1.2	1.7	1.7	1.8	1.6	0.324037
16			1.7	1.9	1.7	1.6	1.68	0.132665
					AVG	1.519333	
					SD	0.11393	

Back end Data Electronics (Processing & Data Acquisition)
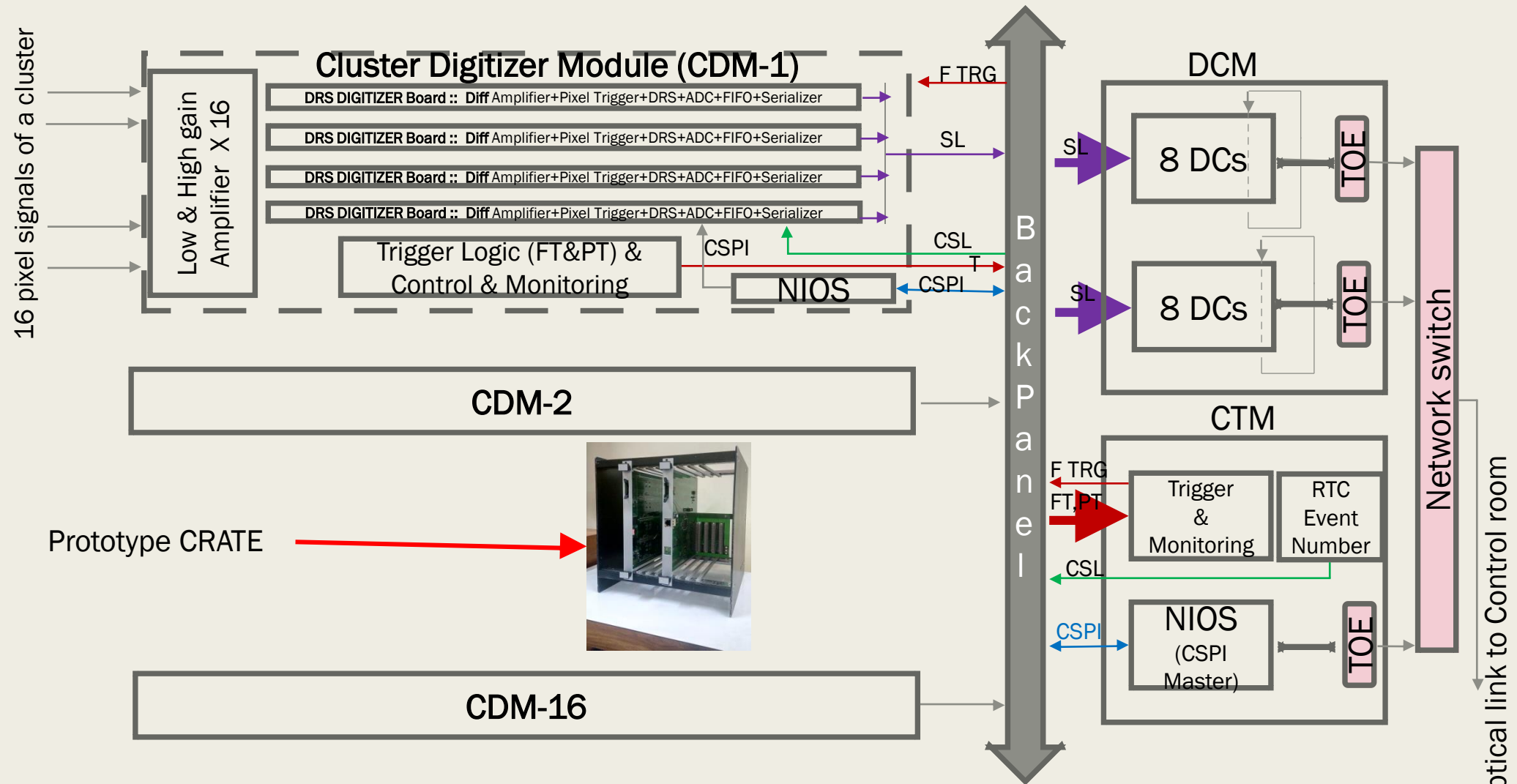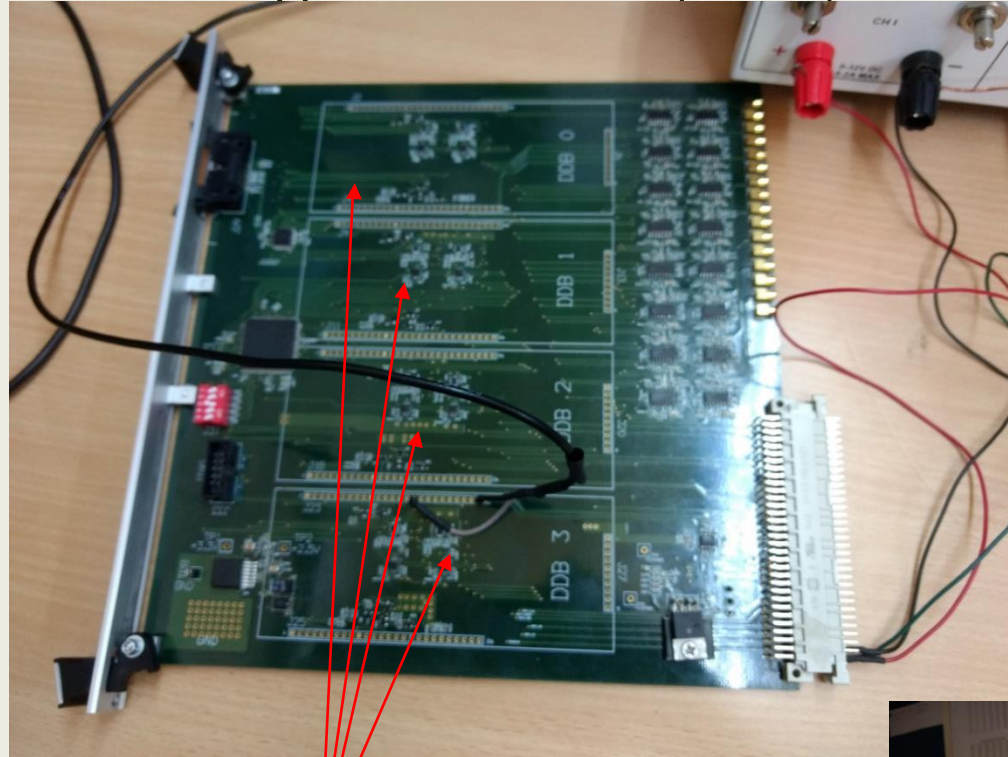

DCM- Data Concentrator Module – houses 4 mezzanine DRS Digitizer Boards (DDB)
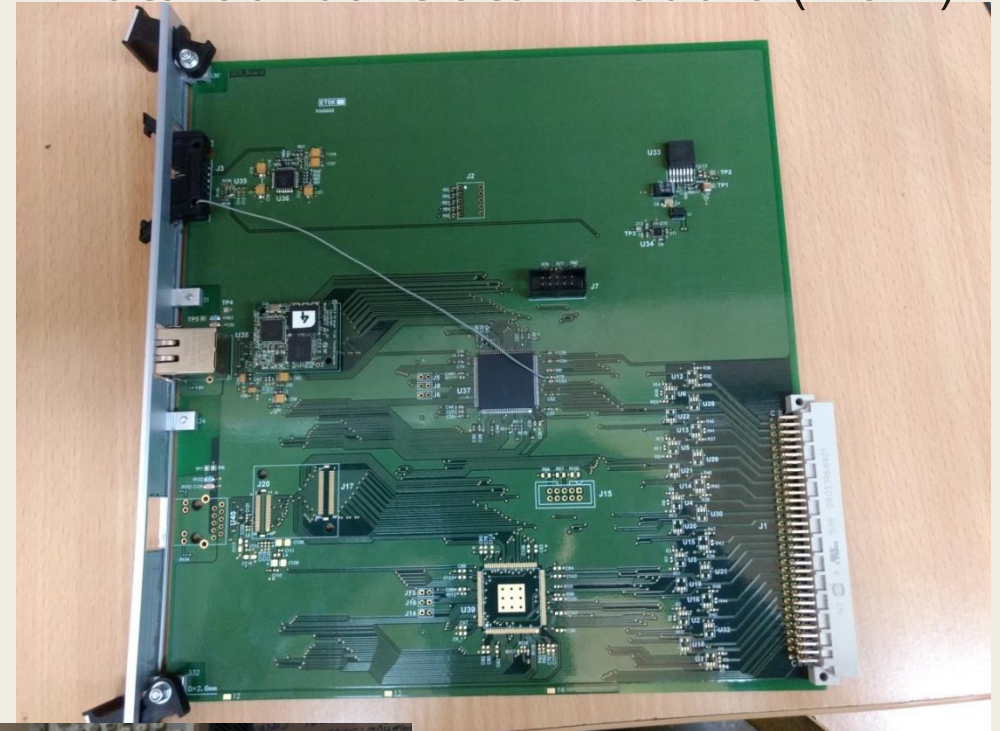CTM- Control & Trigger Module
DRS- 9 chl, 1024 switched capacitor array (analog sampler), 1GSPS , ROI is muxed at Output

Back-end electronics modules
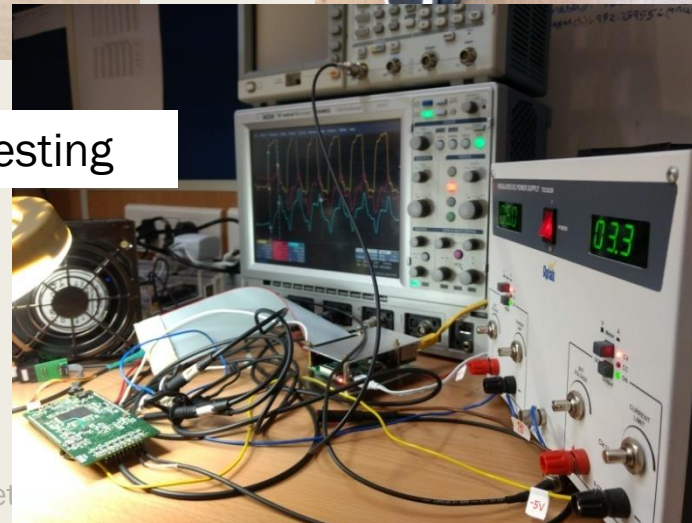
Cluster Digitizer Module (CDM)
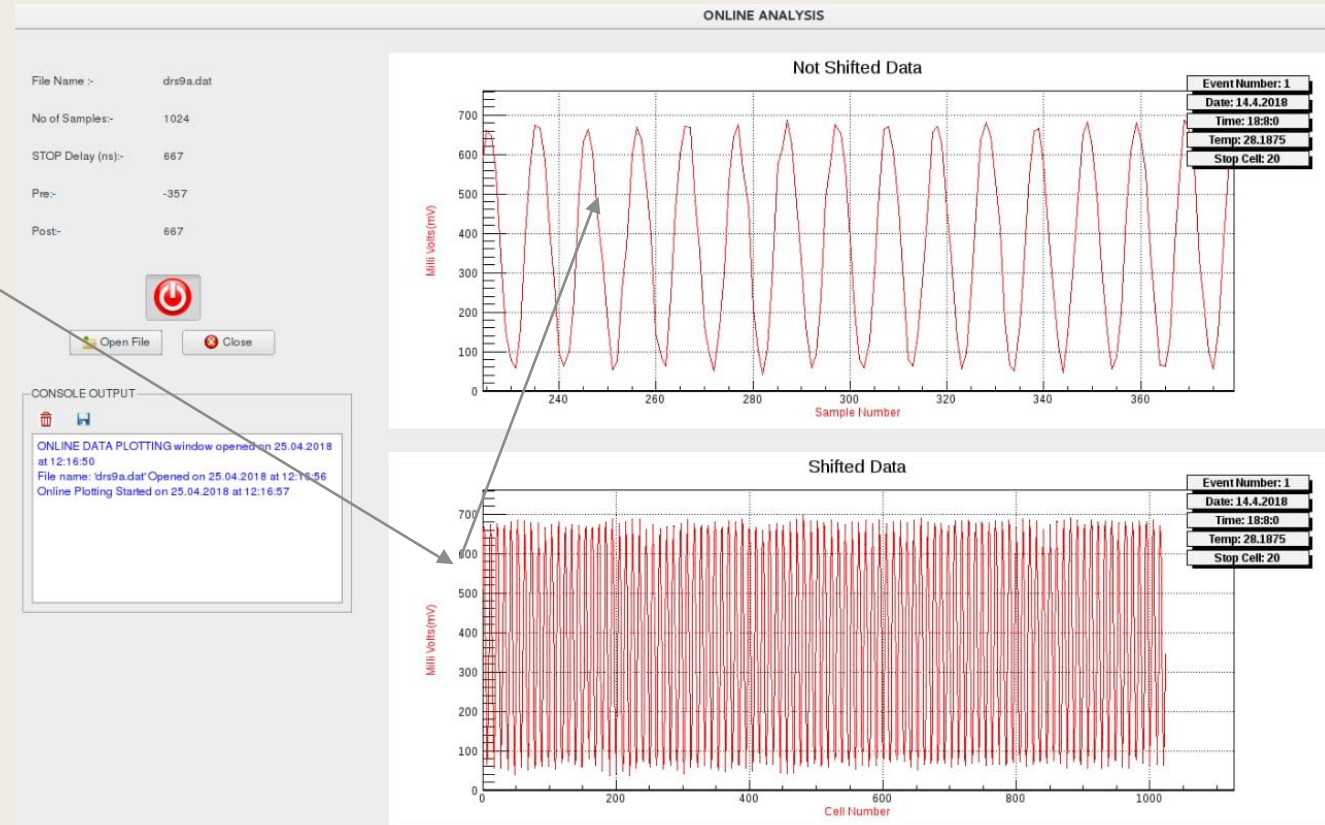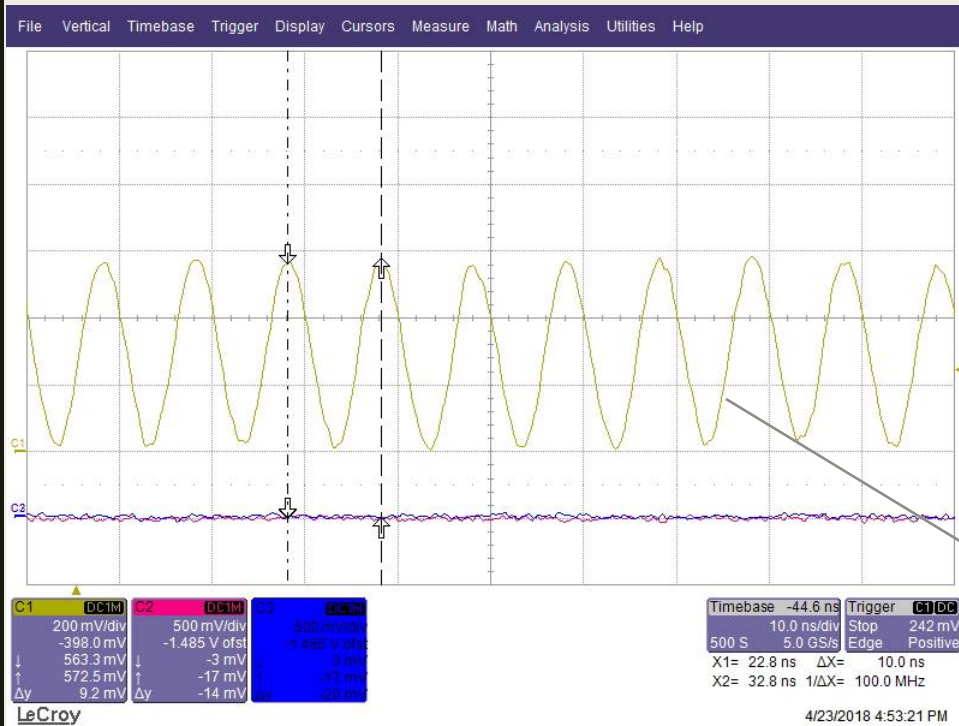
Data Concentrator Module (DCM)

DDB

DDB testing

DDB result- Sine wave sampled @1GSPS

Customized SPI transfer protocol between Hardware modules

■ A customized SPI protocol designed for communication between various modules under Single Master and One or More Slaves scheme. There are basically 3 applications

1. *Raspberry-Pi as Master to control all 32 Bias-boards as slaves*
   - ■ Master and Slave are SW controlled
   - ■ Interface signals :: MOSI,MISO(slave controlled), CLK, nSS, nBSY(optional)
   - ■ nSS invokes Slave interrupt and nSS is active for a complete data transfer cycle . Common or selective slave access.
   - ■ Byte transfer control: Fixed delay of slave latency or nBSY handshake

2. *CTM to CDMs or other modules over back panel CSPI interface*
   - ■ Master and Slave are SW controlled
   - ■ Interface signals: MOSI,MISO(slave controlled), CLK, nSS, nBSY
   - ■ nSS invokes Slave interrupt and nSS is active for complete transfer . Common or selective slave access.
   - ■ Byte transfer control by nBSY signal hand-shake
   - ■ <u>While nSS is inactive, nBSY pulse acts as alert from any slave to Master by invoking interrupt. Master can identify the alerted slaves by issuing common command</u>.

3. *CDM to 4 DDBs : Single slave access*
   - ■ Master is SW controlled and Slave is HW module
   - ■ Interface signals: MOSI,MISO, CLK, nSS and nSS is active for a complete transfer

Trigger, Data throughput and Data Size
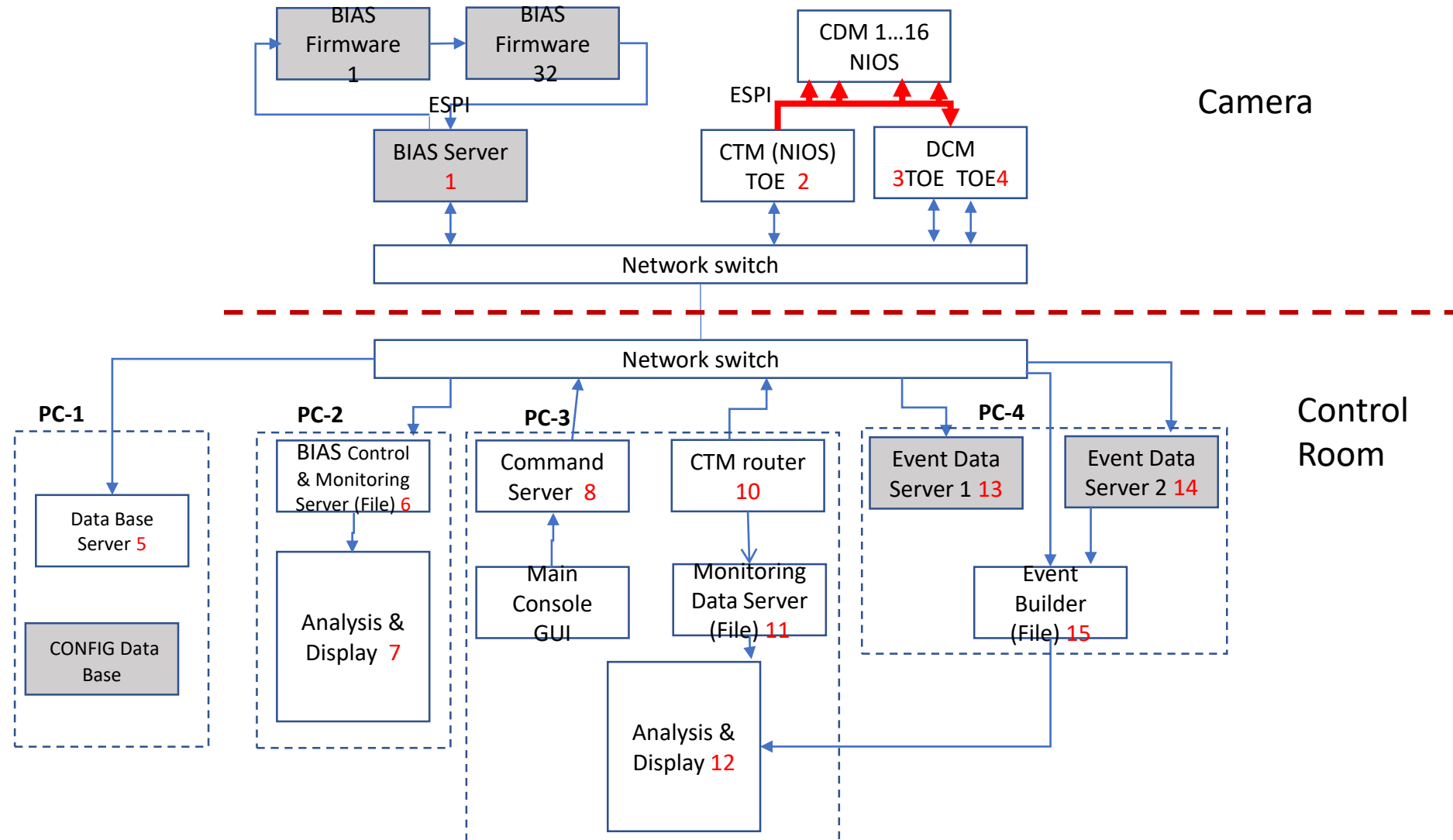
➢ **Trigger logic**
  - ✓ Pixel trigger : Pulse crossing set threshold (programmable)
  - ✓ Full (4 Nearest Neighbours) / Partial (boundary triggers) Triggers in CDM
  - ✓ Partial Triggers across the Pixel Cluster Modules are resolved in CTM
➢ **Trigger rate**
  - ✓ Sampling speed @1GSPS, Region of Interest (ROI) is 100ns
  - ✓ Digitization speed 33 MHz, 14-bit data,
    - ○ Dead time per DDB (4-pixel) 100x30nsx9chl = 27µS+3µS = 30µS, Burst Trigger rate of 33 KHz
    - ○ CDMs to DCM data transfer @ 50 Mbps over 16 dedicated serial LVDS links and pushed to remote data server over two Ethernet links @ 80MBps
    - ○ Event size : 1Mb for ROI of 100ns, Sustained Trigger rate is 800Hz with a data through put of 80MBps
➢ **Data Size for a trigger rate of 50 Hz and Pulse profile of 100ns is 22.5 GB/Hour**

Software Concept
(Data & communication network)

Camera

Control Room

BIAS Firmware 1 → BIAS Firmware 32

CDM 1...16 NIOS

ESPI

BIAS Server 1

CTM (NIOS) TOE 2

DCM 3TOE TOE4

Network switch

Network switch

PC-1

Data Base Server 5

CONFIG Data Base

PC-2

BIAS Control & Monitoring Server (File) 6

Analysis & Display 7

PC-3

Command Server 8

Main Console GUI

CTM router 10

Monitoring Data Server (File) 11

Analysis & Display 12

PC-4

Event Data Server 1 13

Event Data Server 2 14

Event Builder (File) 15

Software status – Configuration data base (Create/Update/View/History)

Software under development
- Event Data Server
- Event Builder

Thank you

Summary of Test runs taken on 04-April 2018

4-GAPDs (pixels) of Pixel Cluster Module (PCM) have been tested along with the cluster digitizer module (CDM). The low/high gain signal (negative pulse) was set as input to CDM unit which gives positive pulse. These pulses were connected directly to VME digitizer setup through 2.5 meters RG174 coaxial cables. The GAPD were operated at 55.0V and temperature was between 24 - 25 degree Celsius.

Figure-8: Pulse charge distribution of 4-subpixels (added) (configured as 1428 upper panel and 8481 lower panel). PX1, PX2, PX3 and PX4 refer to four GAPDs (g1,g2,g3,g4) used in PCM.

Summary of Test runs taken on 04-April 2018

4-GAPDs (pixels) of Pixel Cluster Module (PCM) have been tested along with the cluster digitizer module (CDM). The low/high gain signal (negative pulse) was set as input to CDM unit which gives positive pulse. These pulses were connected directly to VME digitizer setup through 2.5 meters RG174 coaxial cables. The GAPD were operated at 55.0V and temperature was between 24 - 25 degree Celsius.
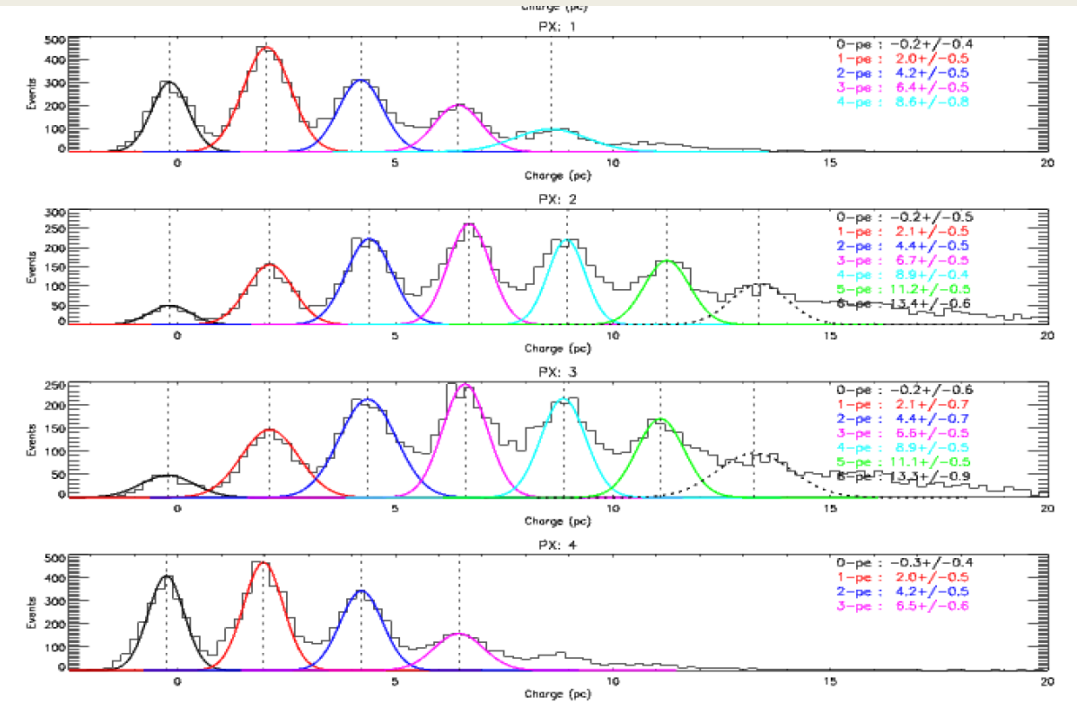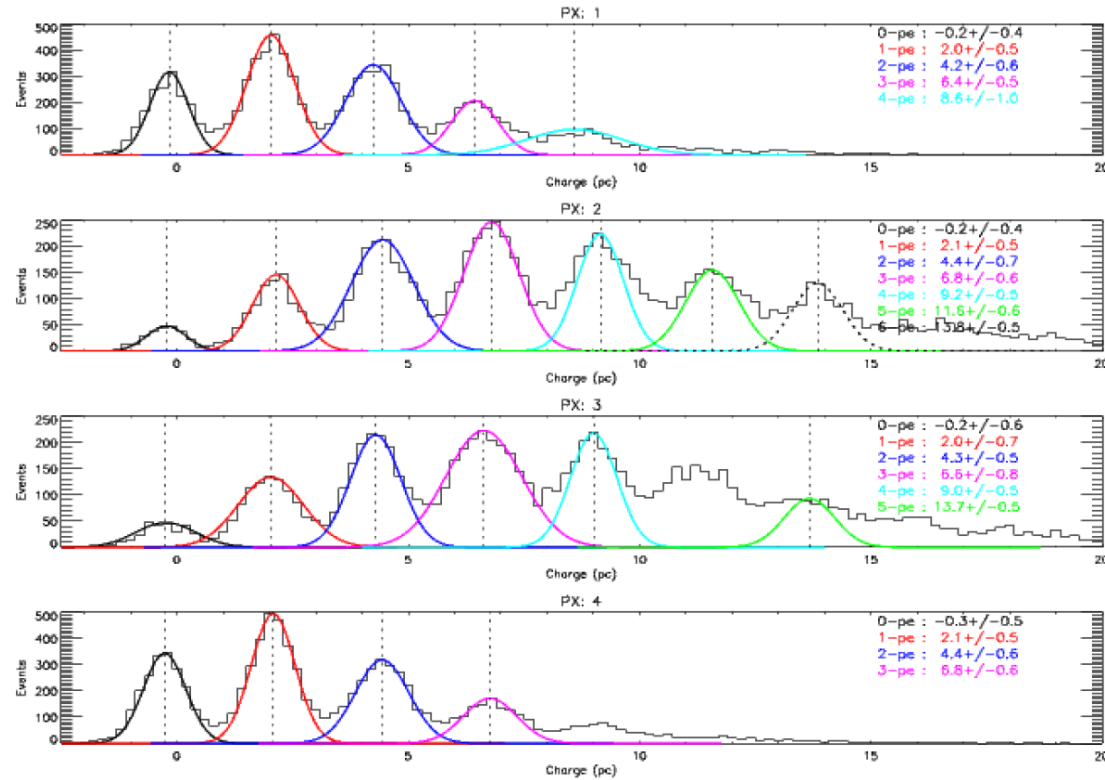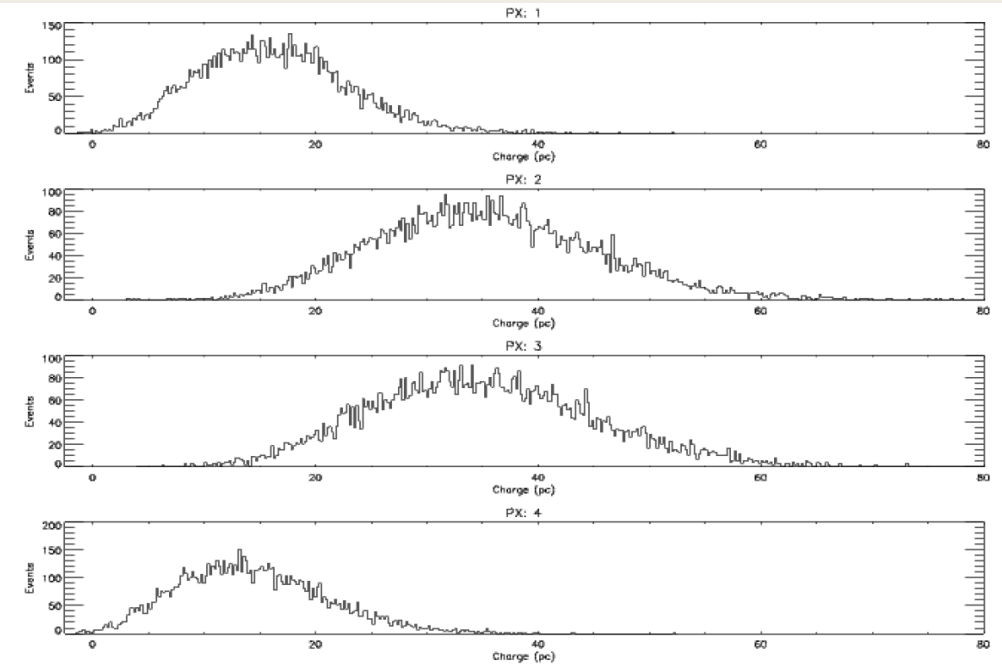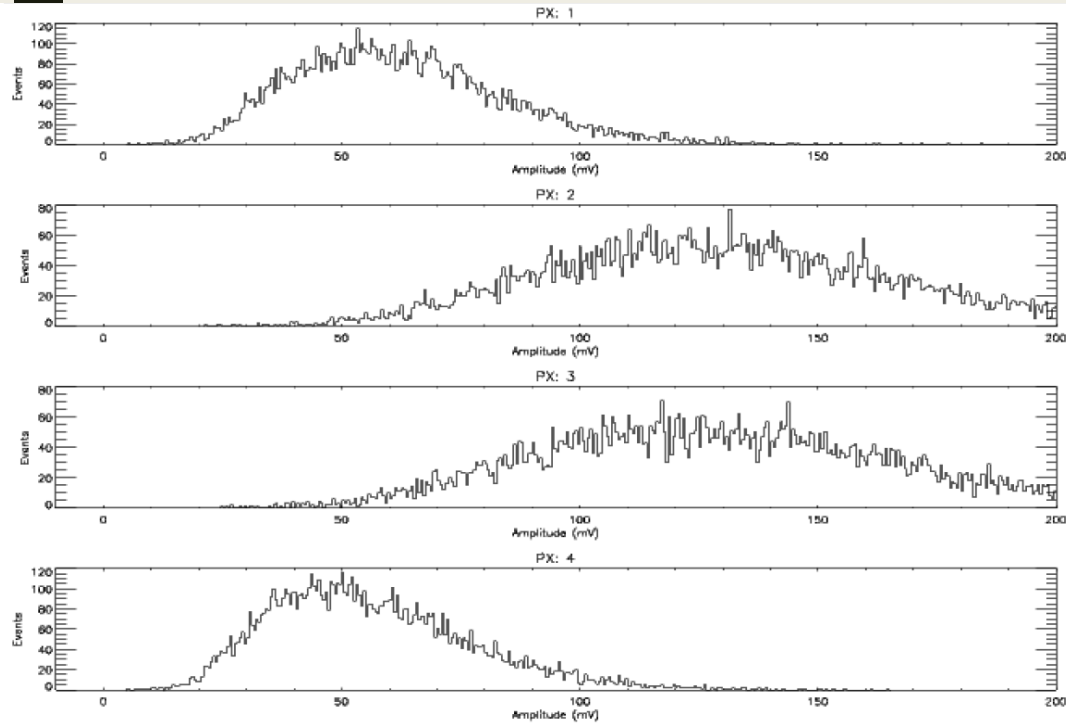

Figure-9: Pulse amplitude and charge distribution of 16-subpixels (added). PX1, PX2, PX3 and PX4 refer to four GAPDs (g1,g2,g3,g4) used in PCM.

General protocol for CSPI

- CSPI –serial protocol is used for communication & data transfer between HW modules in the system
- Single Master – single/multiple Slaves configuration used
- nSS -Invoke interrupt in Slave to initiate the Packet transfer
- First byte is sent after a Slave interrupt latency and Byte transfer with pre defined gap or handshake
- Time out need to be implemented in both Master and Slave
- High priority Commands can be executable immediately or may be executed later in back ground. One can check for command response before reading the result

Interface signals between Master and Slave
- MOSI
- MISO(slave controlled , Wire ANDed and enabled when needed)
- CLK - Typical speed is 100KHz to 1MHz
- nSS – invokes interrupt in slave on –ve edge
- nBSY - used for Byte transfer handshake when nSS is active and when nSS is inactive , nBSY pulse from slave may be used to alert master

Packet Identifier :
bb=00 Individual Slave command
                    bb+C+A+W/r+Bytes(3)
bb=10 Broad cast command to all slaves
                    bb+C+A+W/r+Bytes(3)
bb= 11 ssssss is slave address for selection
bb-= 01 NA
            C=1 : following byte is command
            A=1: following 2 bytes is address H,L
            W/r= 1/0 : Write or read cycle w.r.t
Master
            Bytes (3): =7: following byte represents
                        Data size in bytes
                    =0 to 6 represents no. of data
                        follows
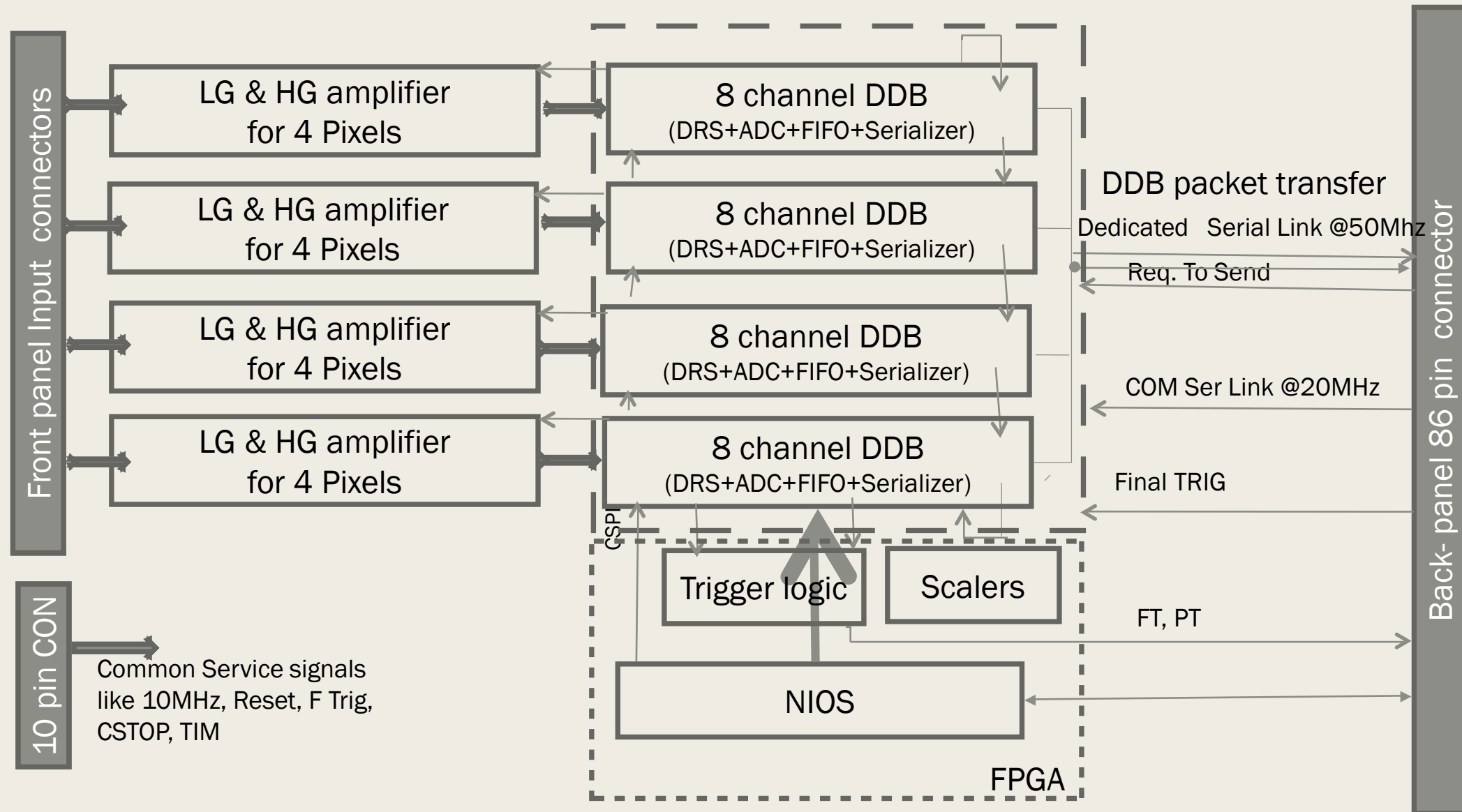If write , checksum will be send at end of data and
check for Success or error received
    if Read, check sum will be send before data and
Success or Fail will be acknowledged
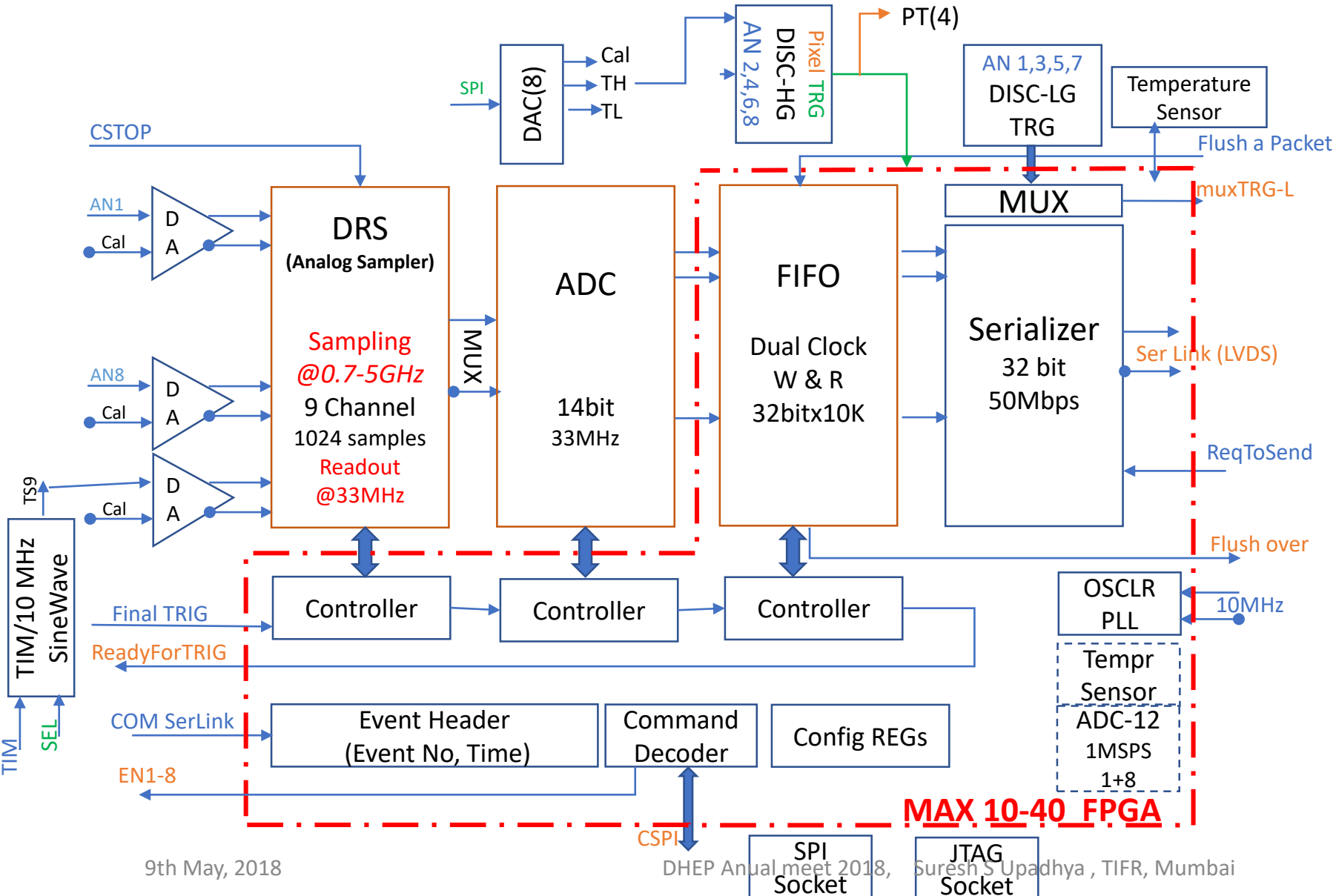Data bytes & check sum is read

Cluster Digitizer Module (CDM)

DRS based Digitizer Board (DDB)

Header
H10: AN1-8
H28x2: Pixel TRG(4)
   Final TRIG
   CSTOP
   COMSerLink-LVDS
   CSPI(5)
   10MHz-LVDS
   ReqToSend
   Flush a Packet
   ReadyForTRIG
   EN1-8
   Flush Over
   SerLinkLVDS
   MuxedTRG-L

DRS Data Packet format (32bit word)
- 0+SFD(15)=0x7BDA+Packet Size(16)
  Packet size= Pre(8W)+Pixel Data(variable)+Post(3W)
  Pixel data =1W + [ROI/2]xNo. Of valid chnls in a DRS
- Compliment word of first except 1st bit
- 0+Event Flags(5) + NU(10)+calibration details(16)
- 0+Event number(31)
- 010+Time stamp in 0.1 usec(29)
- 011+Time stamp in Years(4)+Seconds(25)
- 0b+CDM Position ID(6)+DDB position ID(2)+ DRS temperature(23)
- 0+VCF(9) + LGHG Latch status(8)+CSTOP delay(10)
- {0+Chl ID(4) + STOP cell(10)+skip cells(8)+ROI(9)
  [0+0+BBD ID(2) + Data(14)+Data(14)]xROI(even)%2
  } x Corresponding VCF(9) bits set
- Charge Data for 8 channel (8W=sum of ROI)
- 0+Checksum (2s compl)
- 1+Reserved for packet number by DC
- 1+EFD(15) =0x6DAC+ observed Packet size (counter)

Data Concentrator Module (DCM)
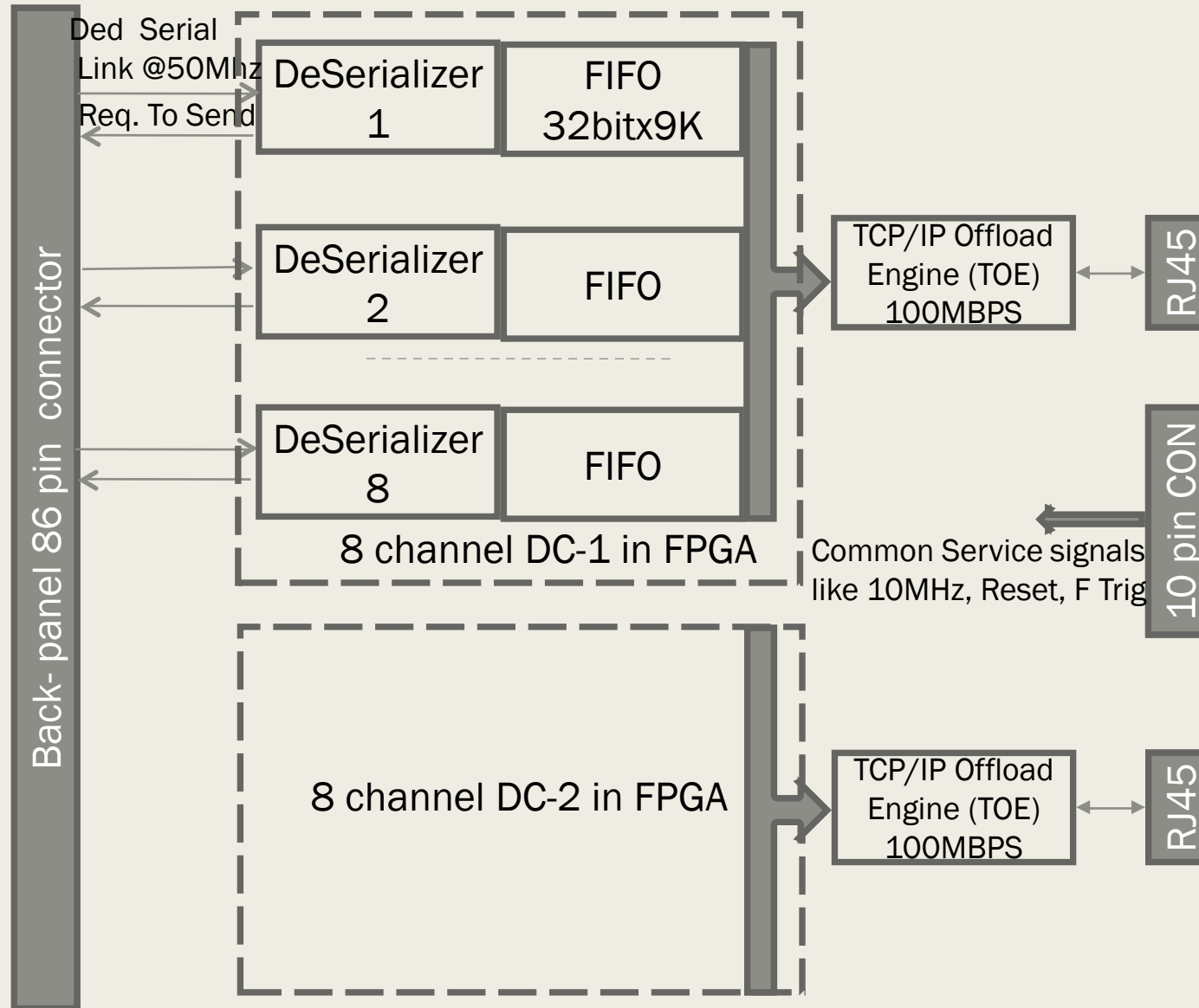
Control & Trigger Module (CTM)
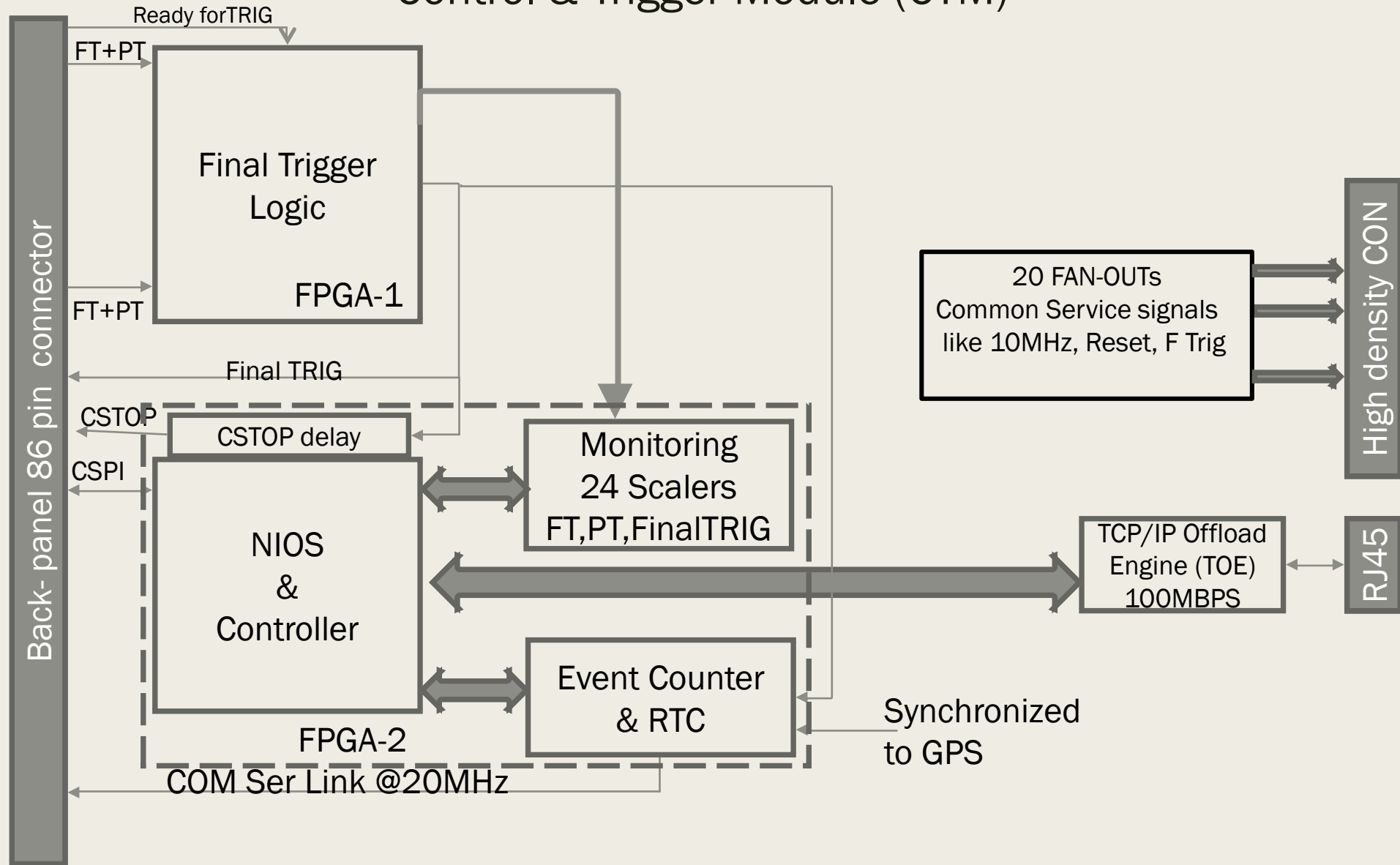
Current Status of Back end

CDM

DDB
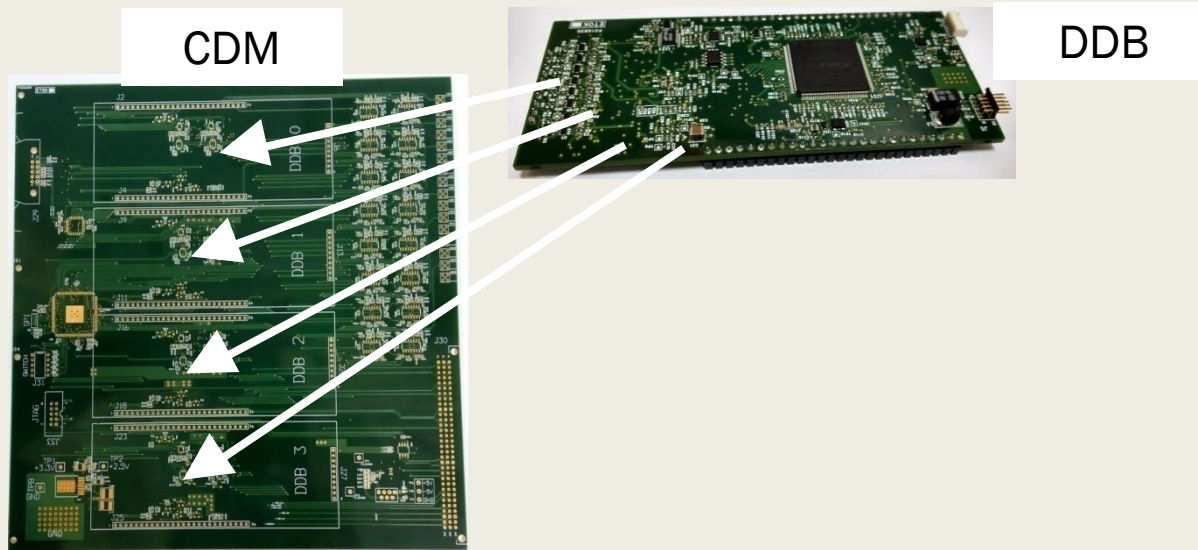
MAX10FPGA Development Board

- CDM board – started assembly
- DDB board – Assembled and being tested
- DCM concept is tested using two Max10 FPGA-Zest ETM development boards
  - Data through-put of 80MBPS is achieved
- CTM NIOS interface to remote PC is tested using Max10 FPGA-Zest ETM development board
- 6 slots prototype of Back panel PCB layout is getting ready
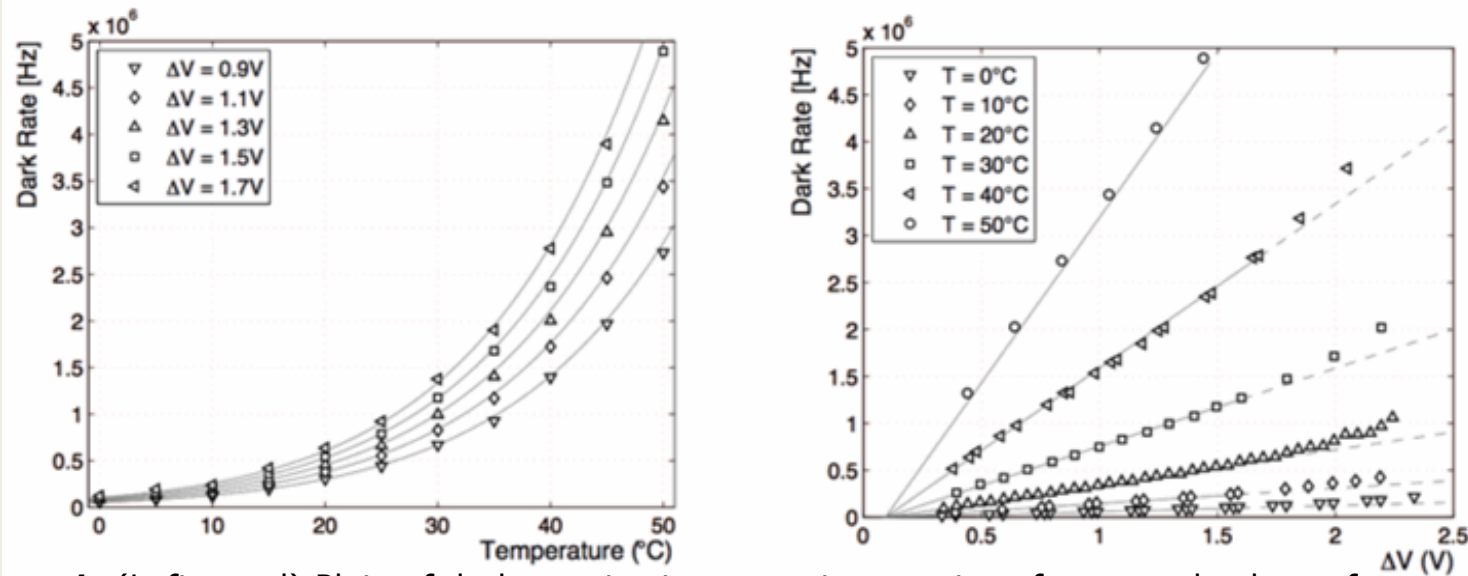
Figure 1. (Left panel) Plots of dark count rate versus temperature for several values of overvoltage. (Right panel) Plots of dark count rate versus overvoltage at several temperatures. Both figures are from Vacheret et al. (2011) for Hamamatsu S10362-11-050C.
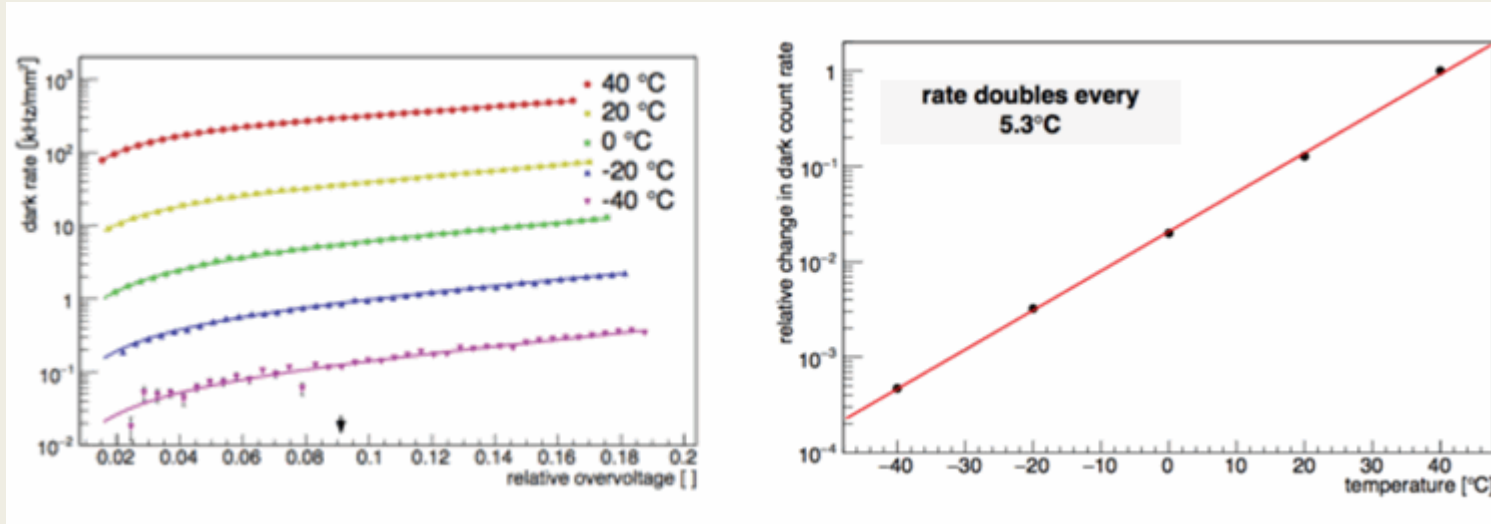
Figure 2. (Left panel) Dark count rate density versus relative overvoltage ($\Delta V/V_{BD}$) for several temperatures. The arrow on the X-axis points to the recommended setting of relative overvoltage. (Right panel) Dark count rate relative to that at 40 °C as a function of temperature at fixed relative overvoltage for Hamamatsu S13360-3050CS SiPM. Source: Otte at al. (2016).

Summary of Test runs taken on 04-April 2018

4-GAPDs (pixels) of Pixel Cluster Module (PCM) have been tested along with the cluster digitizer module (CDM). The low/high gain signal (negative pulse) was set as input to CDM unit which gives positive pulse. These pulses were connected directly to VME digitizer setup through 2.5 meters RG174 coaxial cables. The GAPD were operated at 55.0V and temperature was between 24 - 25 degree Celsius.
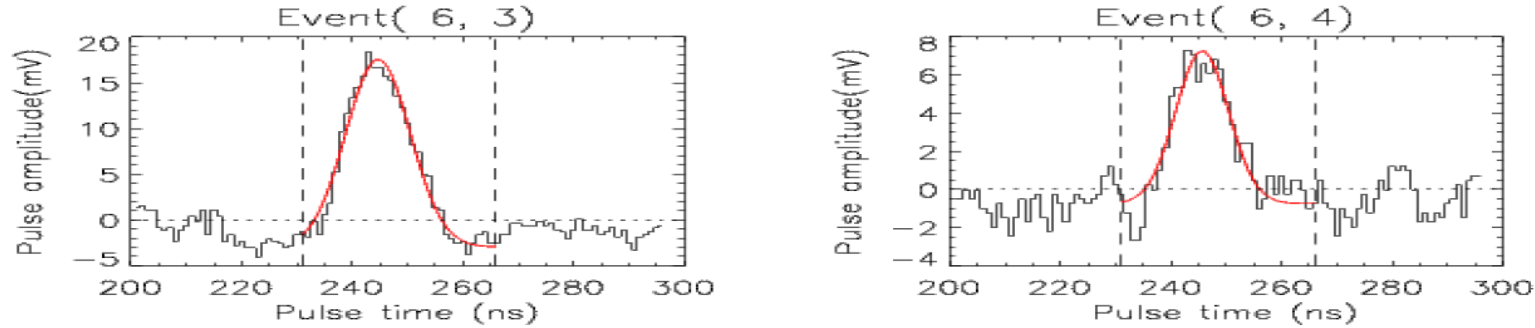
Figure-1: Typical pulse shape of a subpixel from two different GAPD (g3, g4)
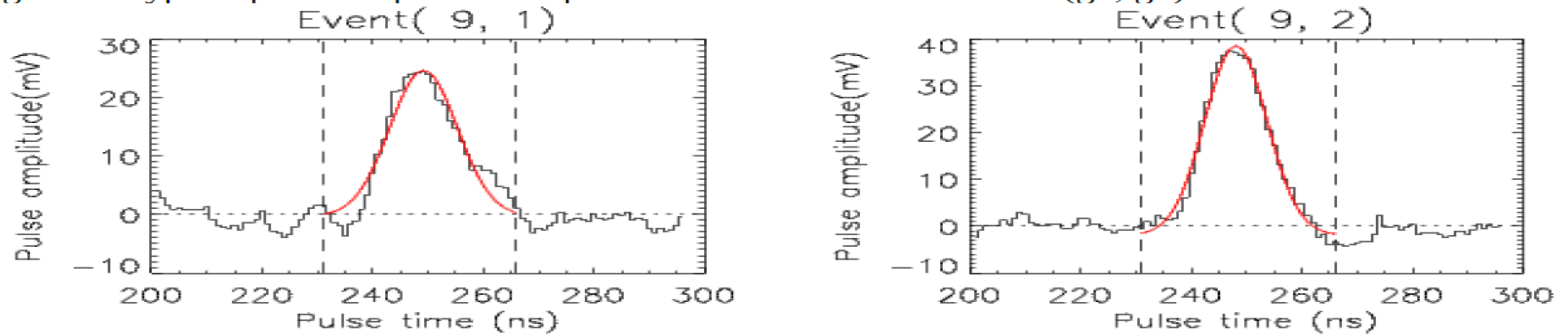
Figure-2: Typical pulse shape of 4-subpixels (added) from two different GAPD (g1, g2)
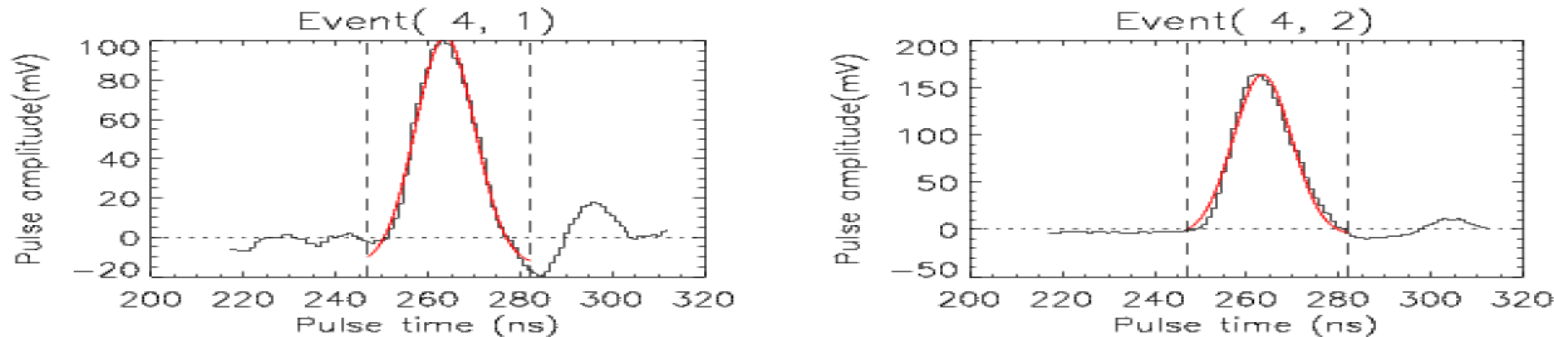
Figure-3: Typical pulse shape of 16-subpixels (added) from two different GAPD (g1, g2)

Summary of Test runs taken on 04-April 2018

4-GAPDs (pixels) of Pixel Cluster Module (PCM) have been tested along with the cluster digitizer module (CDM). The low/high gain signal (negative pulse) was set as input to CDM unit which gives positive pulse. These pulses were connected directly to VME digitizer setup through 2.5 meters RG174 coaxial cables. The GAPD were operated at 55.0V and temperature was between 24 - 25 degree Celsius.

Figure-4: Pulse amplitude and charge distribution of a subpixel (configured as a1). PX1, PX2, PX3 and PX4 refer to four GAPDs (g1,g2,g3,g4) used in PCM.

Summary of Test runs taken on 04-April 2018

4-GAPDs (pixels) of Pixel Cluster Module (PCM) have been tested along with the cluster digitizer module (CDM). The low/high gain signal (negative pulse) was set as input to CDM unit which gives positive pulse. These pulses were connected directly to VME digitizer setup through 2.5 meters RG174 coaxial cables. The GAPD were operated at 55.0V and temperature was between 24 - 25 degree Celsius.


Figure-5: Pulse amplitude and charge distribution of a subpixel (configured as b2). PX1, PX2, PX3 and PX4 refer to four GAPDs (g1,g2,g3,g4) used in PCM.

Summary of Test runs taken on 04-April 2018

4-GAPDs (pixels) of Pixel Cluster Module (PCM) have been tested along with the cluster digitizer module (CDM). The low/high gain signal (negative pulse) was set as input to CDM unit which gives positive pulse. These pulses were connected directly to VME digitizer setup through 2.5 meters RG174 coaxial cables. The GAPD were operated at 55.0V and temperature was between 24 - 25 degree Celsius.
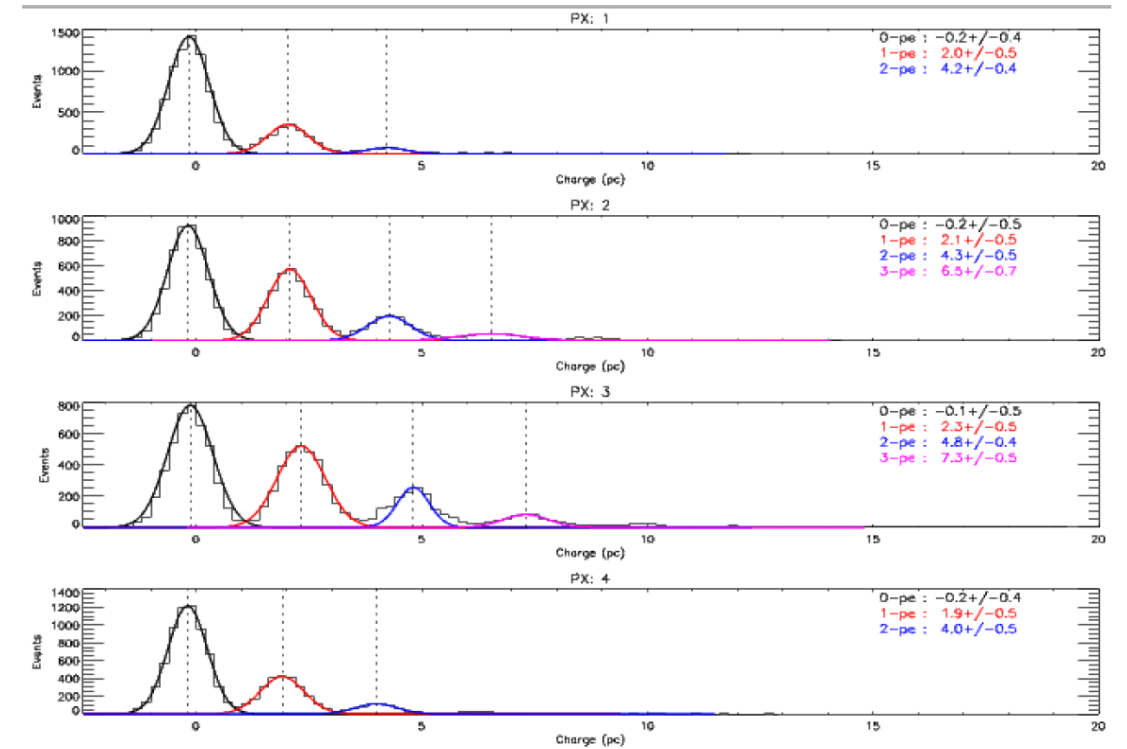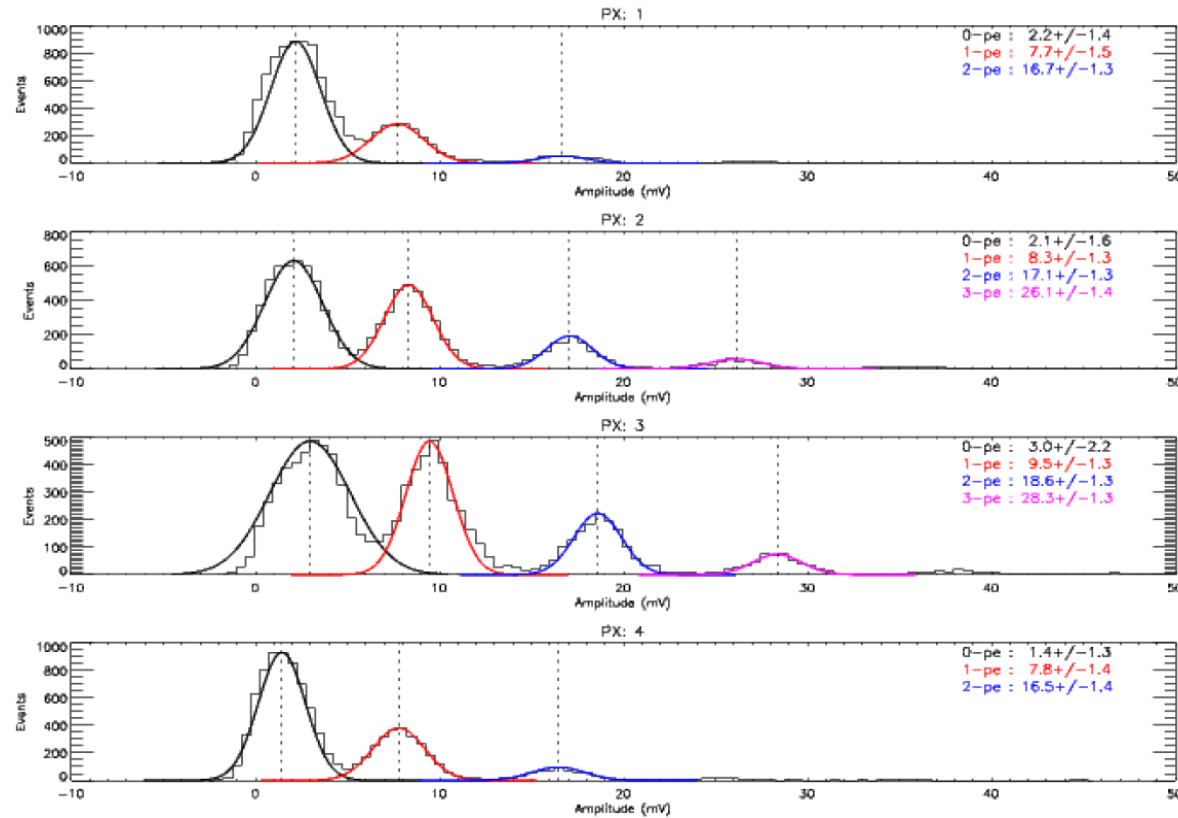

Figure-6: Pulse amplitude and charge distribution of a subpixel (configured as c3). PX1, PX2, PX3 and PX4 refer to four GAPDs (g1,g2,g3,g4) used in PCM.

Summary of Test runs taken on 04-April 2018

4-GAPDs (pixels) of Pixel Cluster Module (PCM) have been tested along with the cluster digitizer module (CDM). The low/high gain signal (negative pulse) was set as input to CDM unit which gives positive pulse. These pulses were connected directly to VME digitizer setup through 2.5 meters RG174 coaxial cables. The GAPD were operated at 55.0V and temperature was between 24 - 25 degree Celsius.
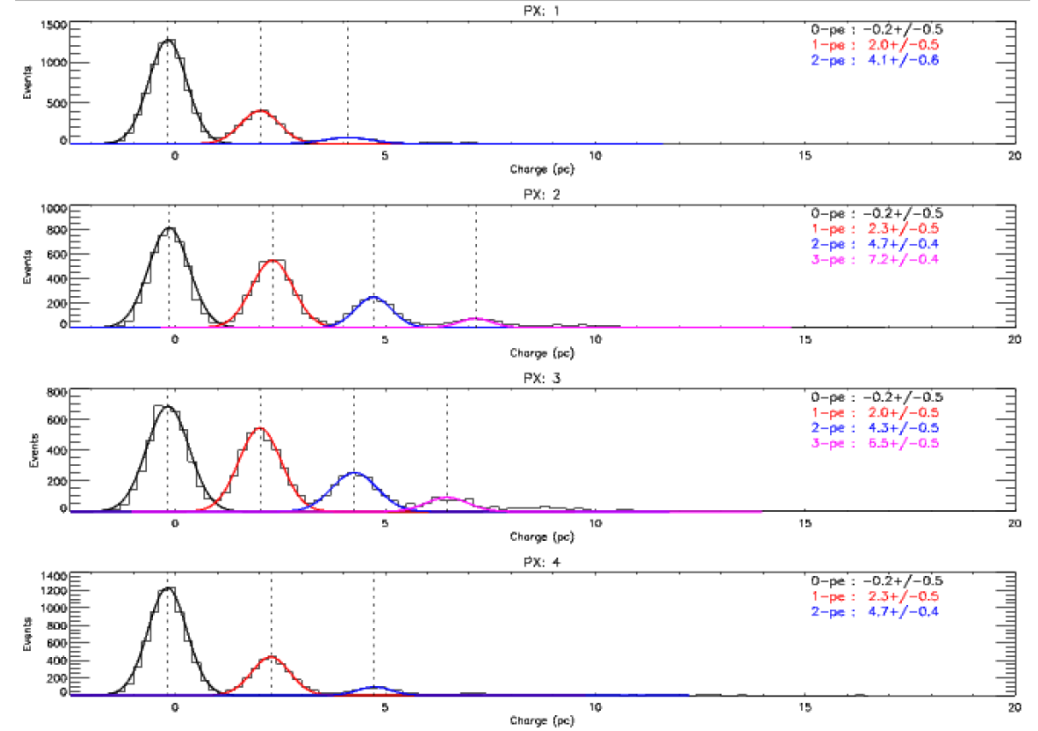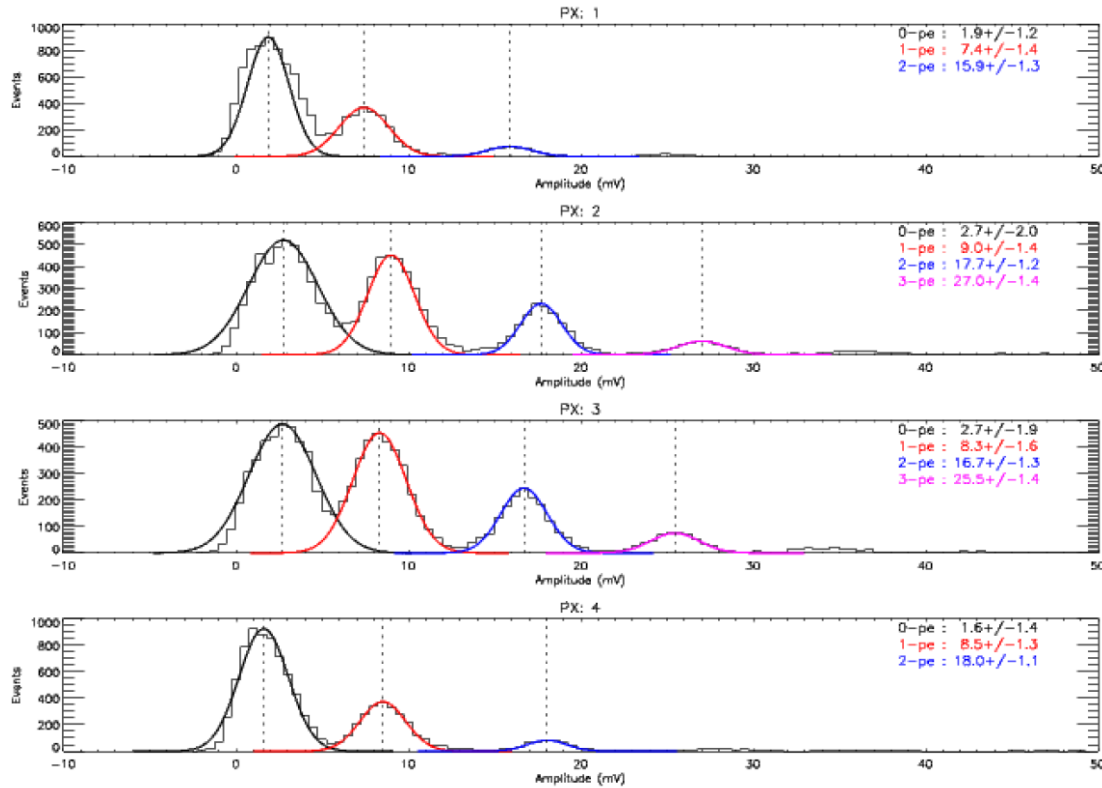

Figure-7: Pulse charge distribution of 4-subpixels (added) (configured as 0660 upper panel and 1248 lower panel). PX1, PX2, PX3 and PX4 refer to four GAPDs (g1,g2,g3,g4) used in PCM.

4-GAPDs (pixels) of Pixel Cluster Module (PCM) have been tested along with the cluster digitizer module (CDM). The low/high gain signal (negative pulse) was set as input to CDM unit which gives positive pulse. These pulses were connected directly to VME digitizer setup through 2.5 meters RG174 coaxial cables. The GAPD were operated at 55.0V and temperature was between 24 - 25 degree Celsius.
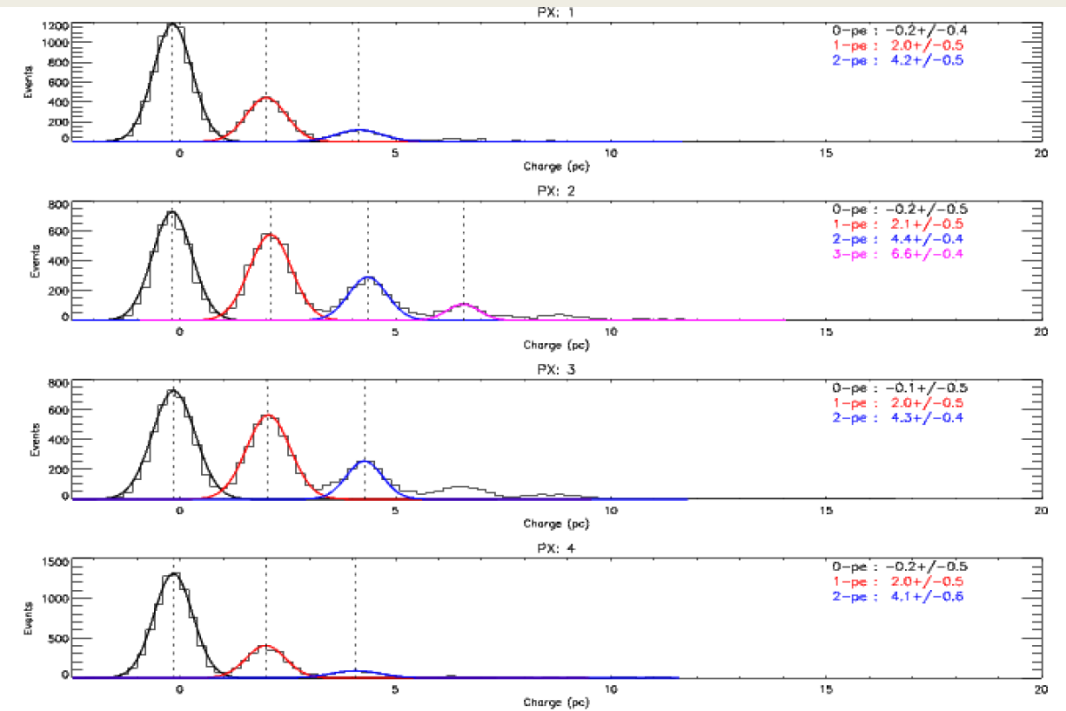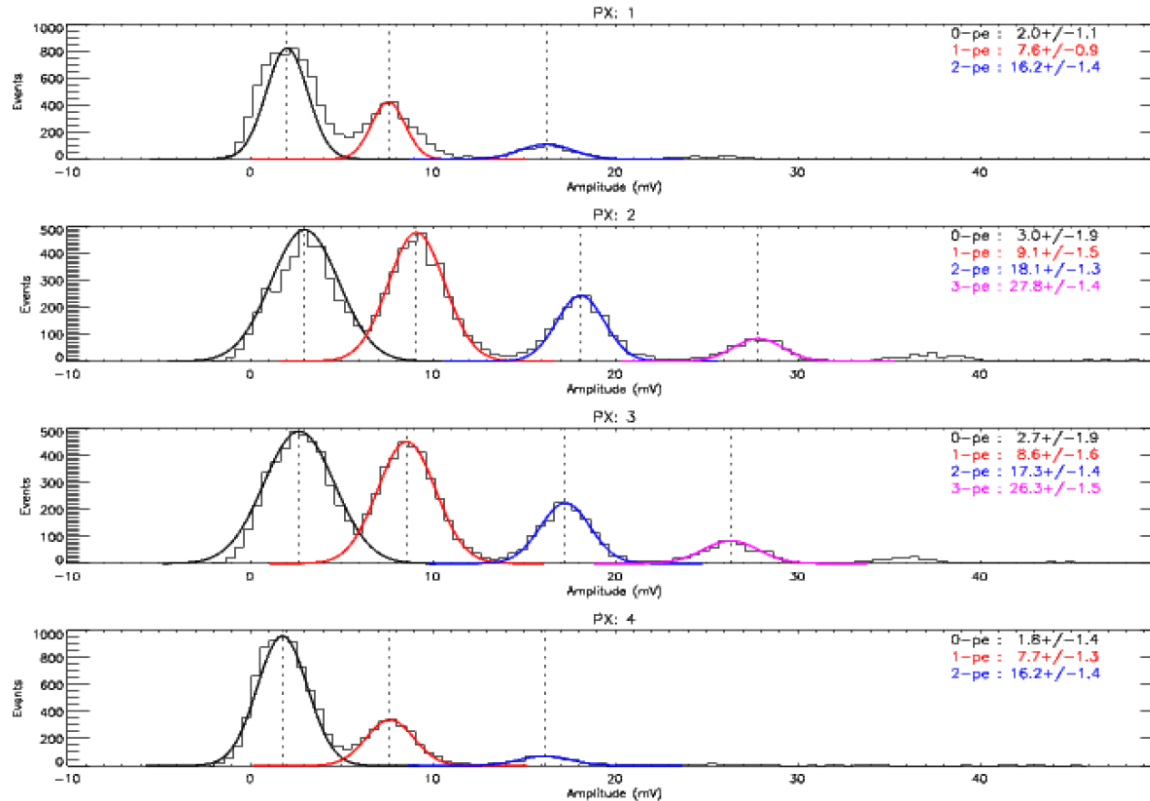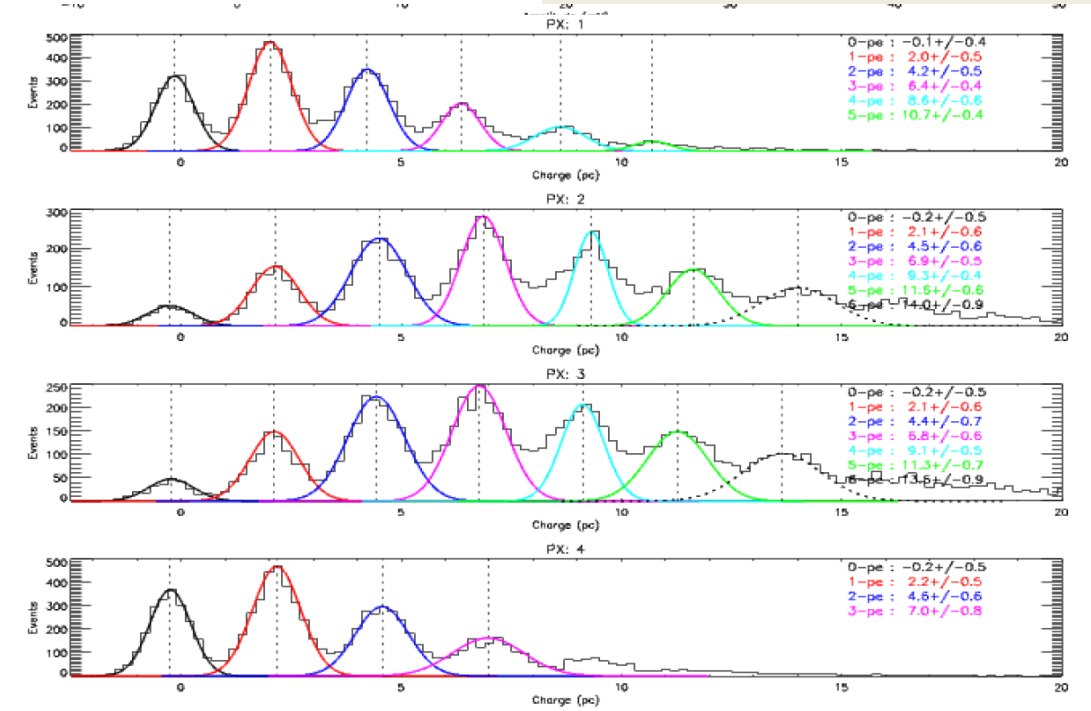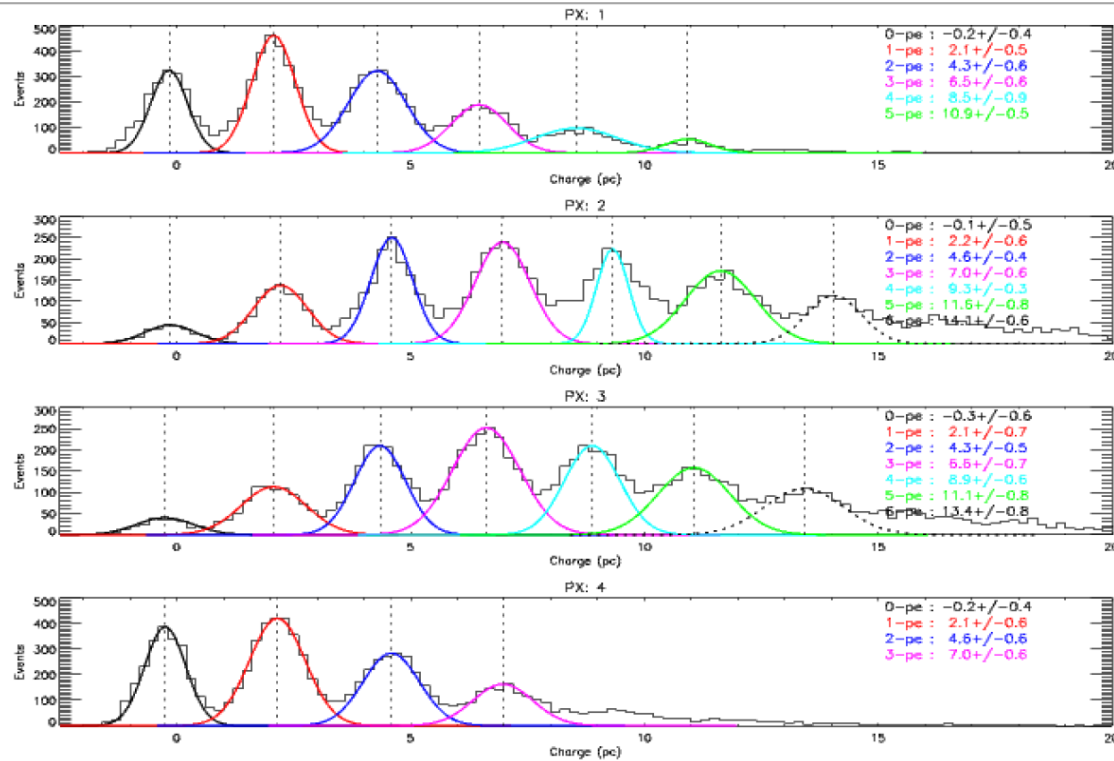
Summary:

(a) Pulse shape of subpixels and added subpixels can be fitted with Gaussian function.

(b) Region of interest (ROI) of 35 ns width with respect to the standard trigger/reference pulse was used to extract amplitude and charge of photoelectrons.

(c) Mean amplitude of pedestal triggers (zero photoelectron) deviates from zero (positive shifted). In case of charge distribution mean pedestal triggers show close to zero value. The mean pedestal value of amplitude or charge measurement must be zero in the absence of light photons (LED off, GAPD Biased below breakdown voltage).

(d) Photoelectron peaks of charge distributions are better than corresponding amplitude distribution.

(e) There is slight variation in the sub-pixel response within a GAPD pixel.

(f) The gain of PX-2 (g2) is slightly higher than others. This could be due to either GAPD characteristic or pixel-chain.

(g) In case of 4-subpixels added response no clear separation between photoelectron peaks of amplitude distribution while charge distribution show clear separation.

(h) In case of of 16-subpixel added response no clear separation between photoelectron peaks of amplitude and charge distribution.

Cost Estimation

1. Cost Amplifier card x 4no....   18400   (7000 reduction) x4

■   Bias card x 2no .....   50000 (HV80=45K) x2

■   ....   15000 (LT3482)x2

■   Power supply card   3000

■   GAPD card ....   8000(2000 Assembly)

■   ---

■   Pixel Cluster Module 184600 ie 11538 per pixel

■   --

2. Cluster Digitizer Module

■   DDB ..... X 4   21000x4

■   CDM   5000

■   -------------------------

■   Total............   89000 ie 5562/pixel

3. Other Modules

■   CTM ...   15000

■   DCM 20000

4. Power supply + crate .. 50000 + 250000

5. Total cost of DAQ Electronics excluding sensor .....   47,12,300 or 35,92,600

   Cost per pixel is   18400 (17000) or 14000(12600)

Software

1. BIAS firmware:
   - *Firmware Initialization*
     - Channel Calibration constants (DAC & ADC), Board ID
   - *Pixel configuration Data (8 Pixels) from Bias Server*
     - Temp- coeff , current coeff, Gain-over voltage constants
     - Bias parameters – Voltage Range, Current limit, Temp range etc
   - *Temperature and current compensation Loop*
   - *Monitoring (8 pixels)*
     - Bias voltage, current, GAPD Temp, Bias Temp
   - *Response to Bias Server commands*
     - Run control data
       - *Pixel Bias ON/OFF, Sub pixel ON/OFF*
       - *Required gain*

Software

2. Data Server
- – *There will be two independent event data servers which is receiving event data packets from two Data concentrators in DCM over ethernet and storing in two Data Buffers. These buffers are shared by the event builder*

3. Event Builder:
- – *Collate data packets from data servers buffer using linked list buffer with N events(based on event no or time). Write data into event file.*

4. Main Console
- – *It is the main Run Console with error window, command buttons*

5. Command Server
- – *Commands received from Main console is formatted suitably in packet and send to CTM router*

6. Monitor Data Server:
- – *The monitoring Data packets received from CTM router is collated and stored in monitoring file.*
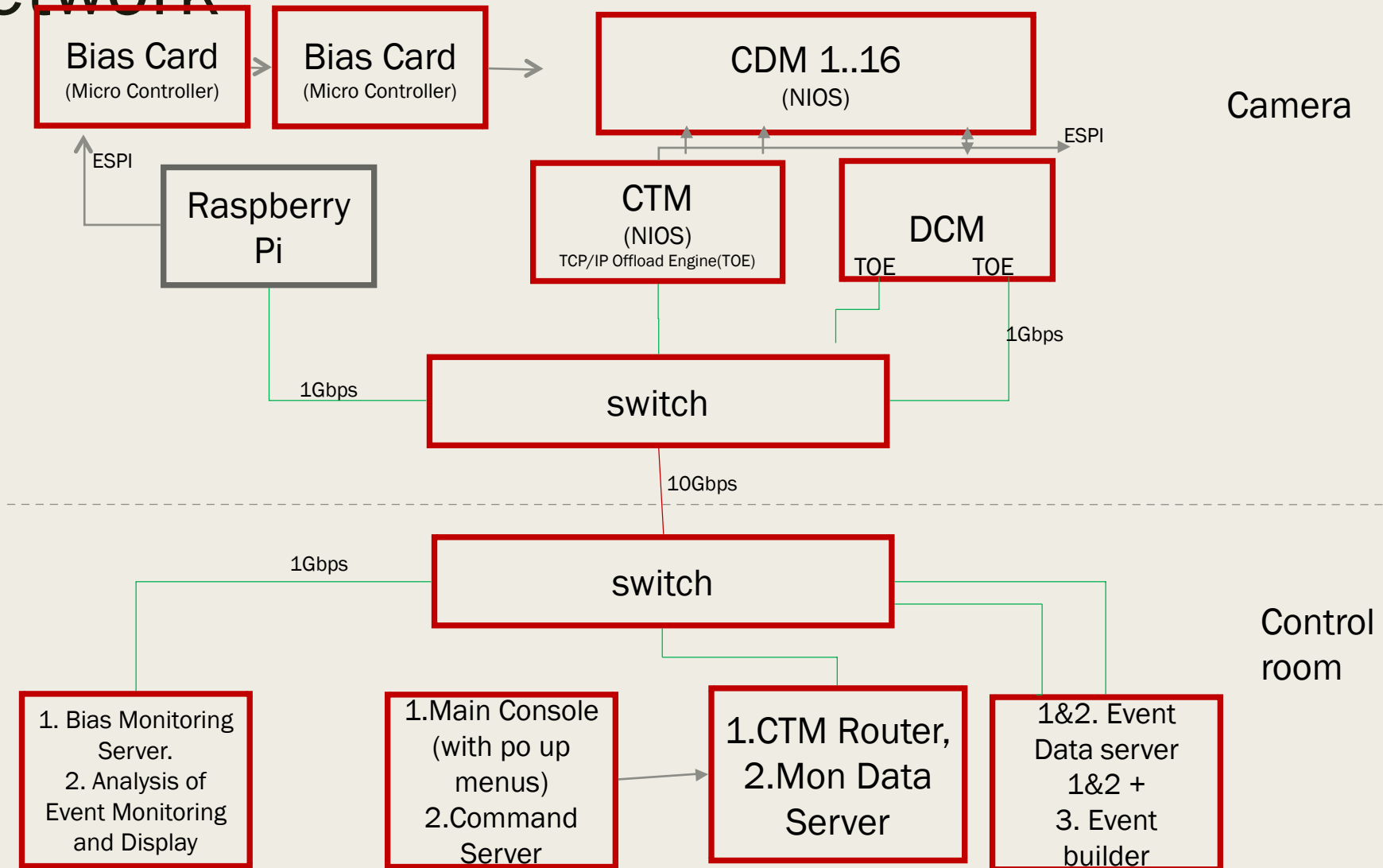
7. CTM router
- – *It is an interface between CTM and Command & Monitoring servers. It suitably packs data compatible to CTM with proper protocol for data transfer.*

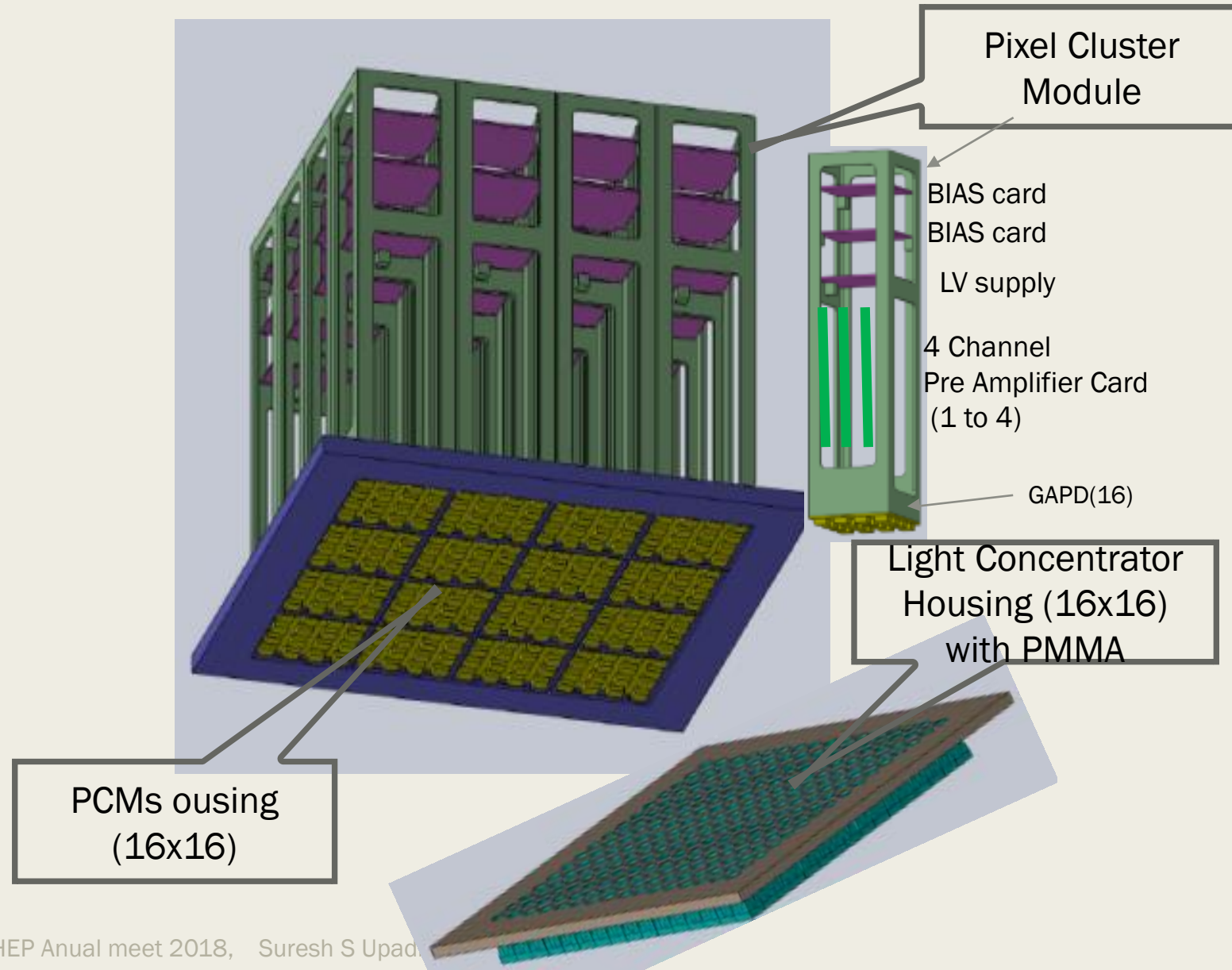8. Event – Monitor Data Analysis with proper displays as well as option of selections.
- – *Online Analysis is done on both the files and displayed GUI based results. User can also execute specific jobs as when necessary*
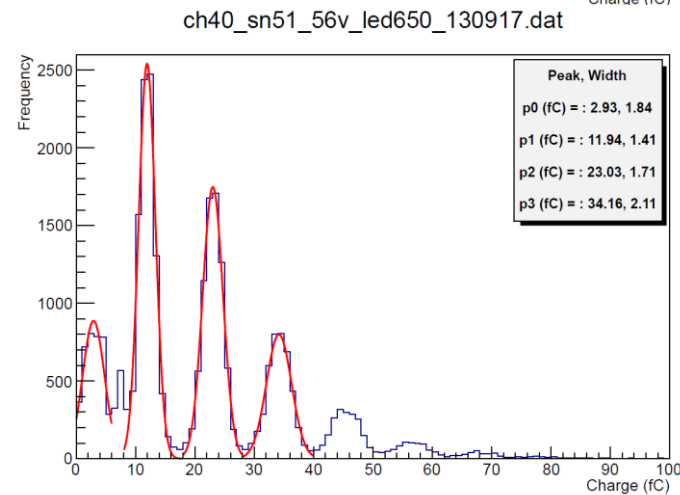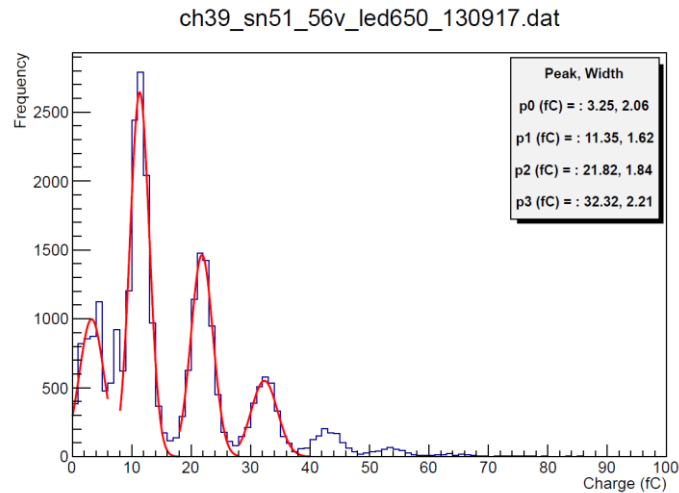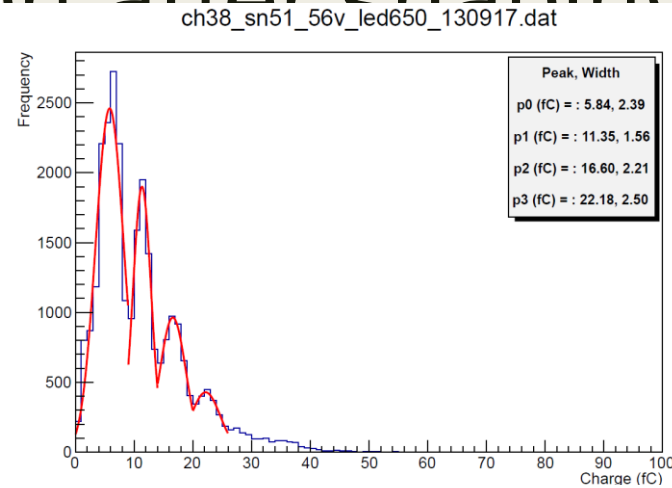
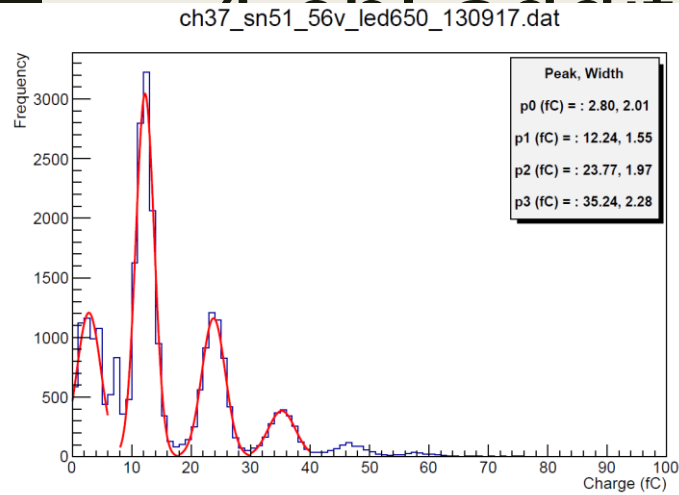# Network

Charge

Camera Electronics

Pixel Cluster Module

BIAS card
BIAS card

LV supply

4 Channel
Pre Amplifier Card
(1 to 4)

GAPD(16)

Light Concentrator
Housing (16x16)
with PMMA

PCMs ousing
(16x16)

Camera Electronics components

- *Camera Electronics front end*
  - Pixels Cluster Module -16no.s
    - *GAPD PCB*
    - *Pre-Amplifier Card – 4no.s*
    - *Bias Supply-2no.s*
    - *LV Supply*
- *Back end Processing & Data Acquisition*
  - 16 Cluster Digitizer Module – 16nos.
    - *DRS Digitizer Board(DDB)– 4no.s in each CDM*
  - Data Concentrator Module- 1no.
  - Trigger & Control Module -1no.
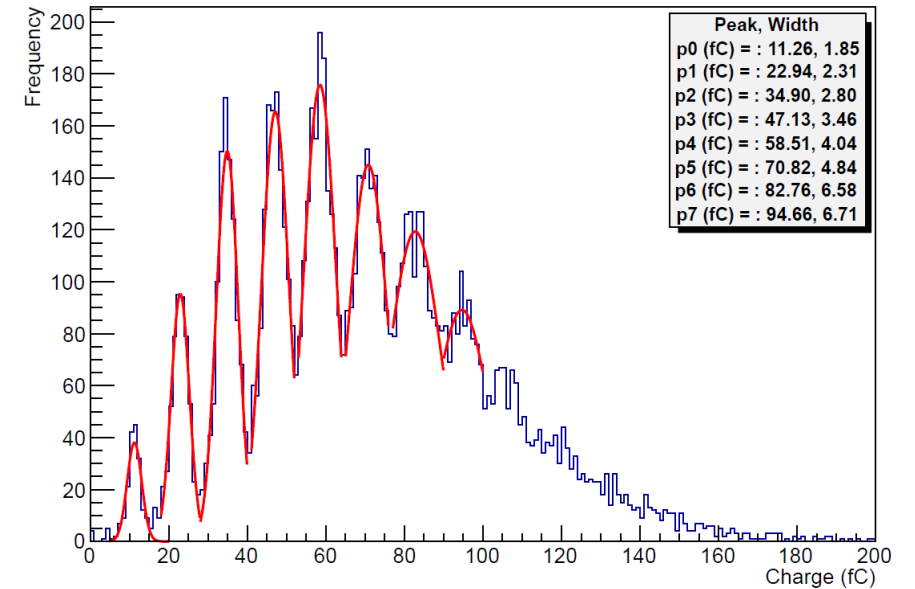 - Bias Server -1 no.

4 Sub Pixel Addition after

4ch_sn51_56v_led650_130917.dat

4 chl addition after shaping (Charge)

ch37_sn51_56v_led650_130917.dat

Peak, Width
p0 (fC) = : 2.80, 2.01
p1 (fC) = : 12.24, 1.55
p2 (fC) = : 23.77, 1.97
p3 (fC) = : 35.24, 2.28

ch38_sn51_56v_led650_130917.dat

Peak, Width
p0 (fC) = : 5.84, 2.39
p1 (fC) = : 11.35, 1.56
p2 (fC) = : 16.60, 2.21
p3 (fC) = : 22.18, 2.50

ch39_sn51_56v_led650_130917.dat

Peak, Width
p0 (fC) = : 3.25, 2.06
p1 (fC) = : 11.35, 1.62
p2 (fC) = : 21.82, 1.84
p3 (fC) = : 32.32, 2.21

ch40_sn51_56v_led650_130917.dat

Peak, Width
p0 (fC) = : 2.93, 1.84
p1 (fC) = : 11.94, 1.41
p2 (fC) = : 23.03, 1.71
p3 (fC) = : 34.16, 2.11

4ch_sn51_56v_led650_130917.dat

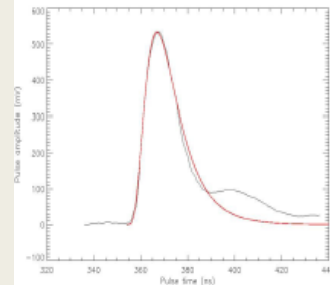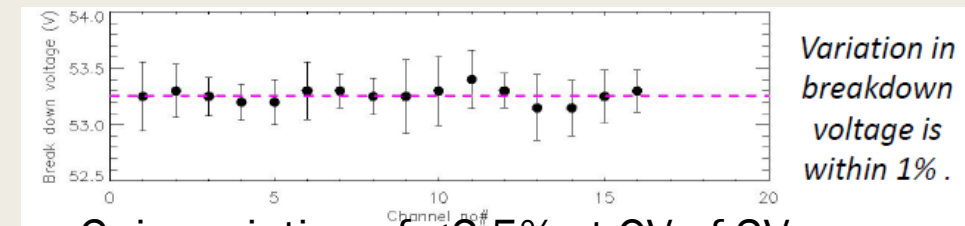| Peak, Width |
|---|
| p0 (fC) = : 11.26, 1.85 |
| p1 (fC) = : 22.94, 2.31 |
| p2 (fC) = : 34.90, 2.80 |
| p3 (fC) = : 47.13, 3.46 |
| p4 (fC) = : 58.51, 4.04 |
| p5 (fC) = : 70.82, 4.84 |
| p6 (fC) = : 82.76, 6.58 |
| p7 (fC) = : 94.66, 6.71 |

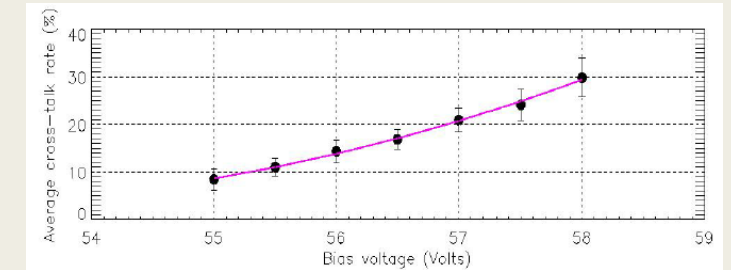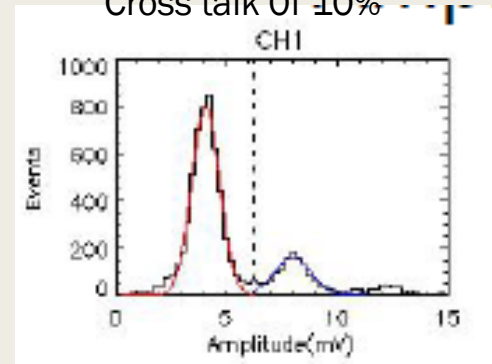# Characterization of Hamamatsu S13361-3050AS-04
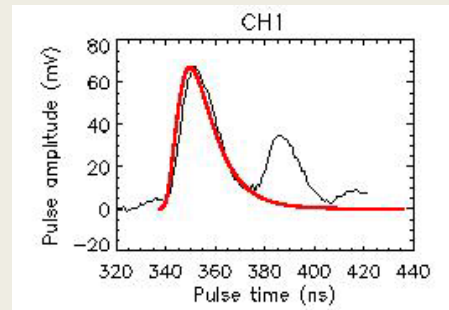
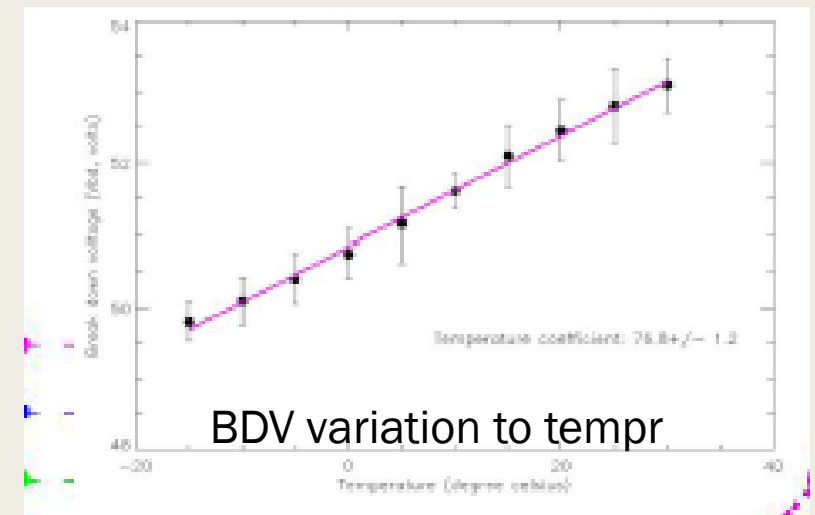Pulse shape of sum of 16-channel in a 4x4 GAPD array
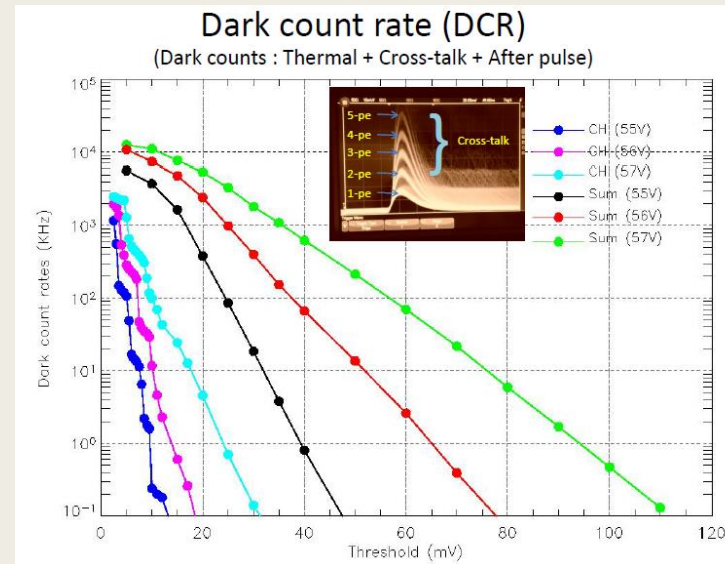

- Rise time : 7 ~ 8 ns
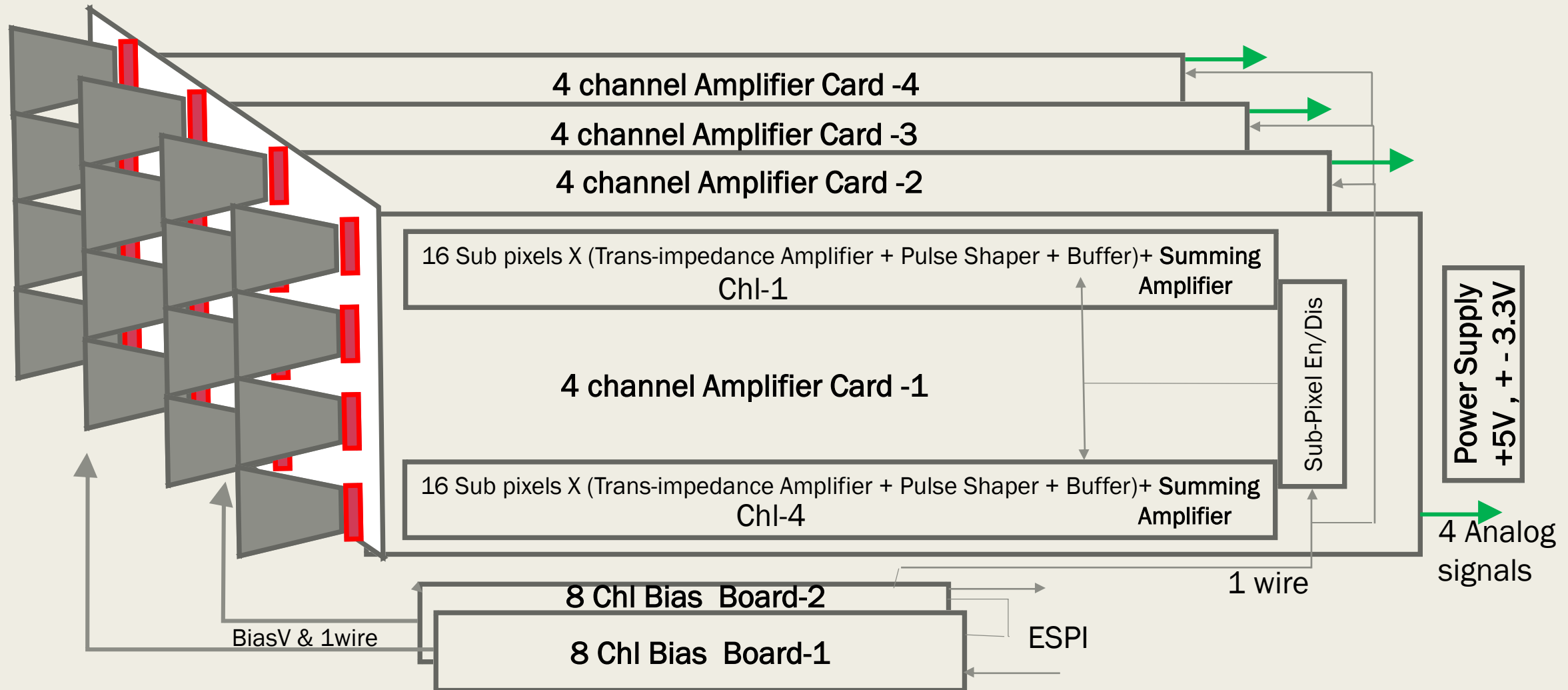- Fall time : 25 ~ 30 ns
- FWHM : 17 ~ 20 ns
- Time jitter : 1 ~ 2 ns

Cross talk 0f 10%

Variation in breakdown voltage is within 1% .

Gain variation of <2.5% at 0V of 3V

Dark count rate (DCR)
(Dark counts : Thermal + Cross-talk + After pulse)

BDV variation to tempr

Pixel Cluster Module

4 channel Amplifier Card -4

4 channel Amplifier Card -3

4 channel Amplifier Card -2

16 Sub pixels X (Trans-impedance Amplifier + Pulse Shaper + Buffer)+ **Summing Amplifier**
Chl-1

4 channel Amplifier Card -1

16 Sub pixels X (Trans-impedance Amplifier + Pulse Shaper + Buffer)+ **Summing Amplifier**
Chl-4

Sub-Pixel En/Dis

Power Supply +5V , + - 3.3V

4 Analog signals

1 wire

8 Chl Bias Board-2

8 Chl Bias Board-1

BiasV & 1wire

ESPI
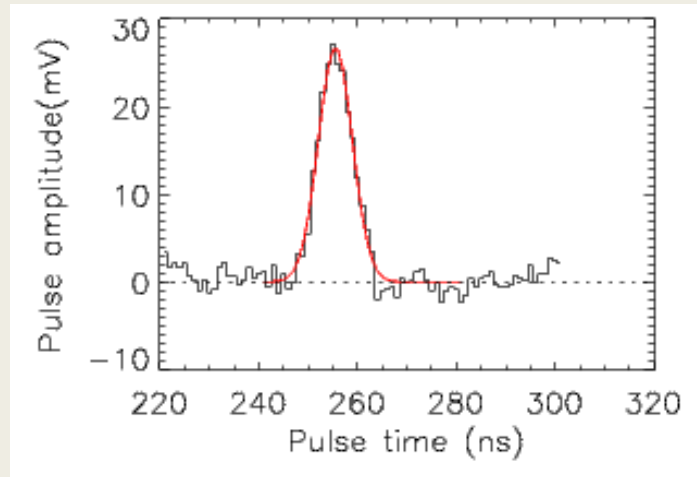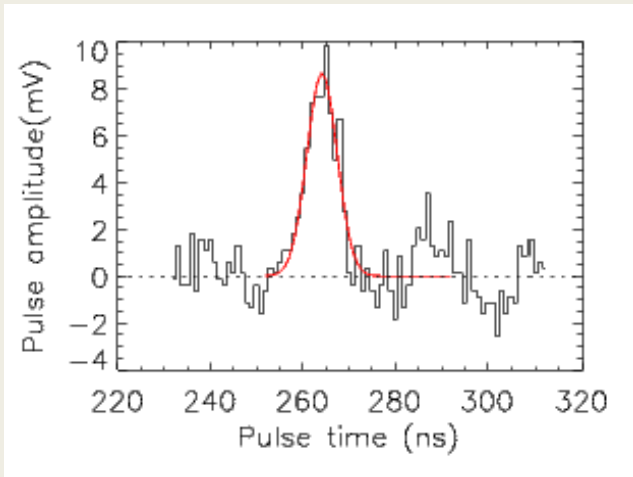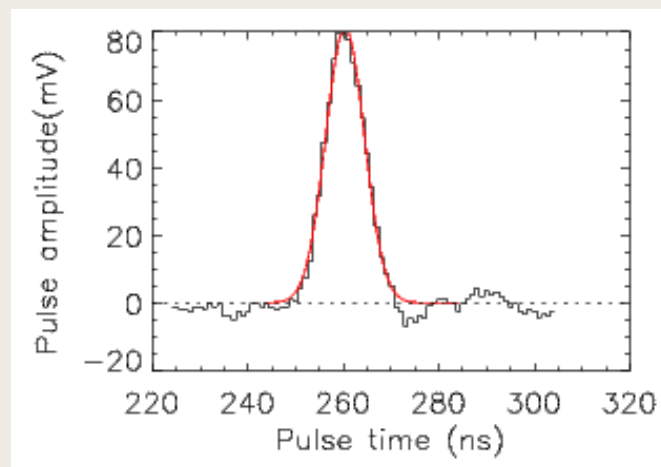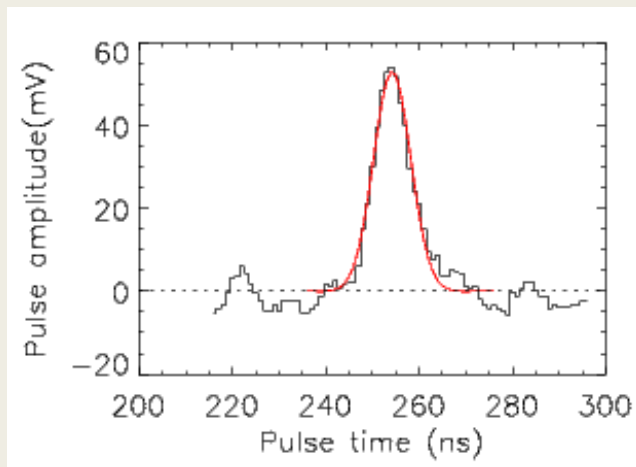
G-APD Pulses of High Gain Channel

Single sub-pixel enabled in a Pixel Amplifier 1/10/18

4 Pixels Amplifier card

All 16 sub-pixels enabled in a Pixel Amplifier

Amplifier with test ZIG & CDM