Current Status of Back-end Electronics for GAPD based Imaging Camera

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Back-end Electronics

Back-end Electronics Modules

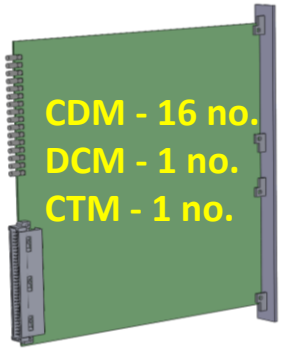
Cluster Digitizer Module (CDM)

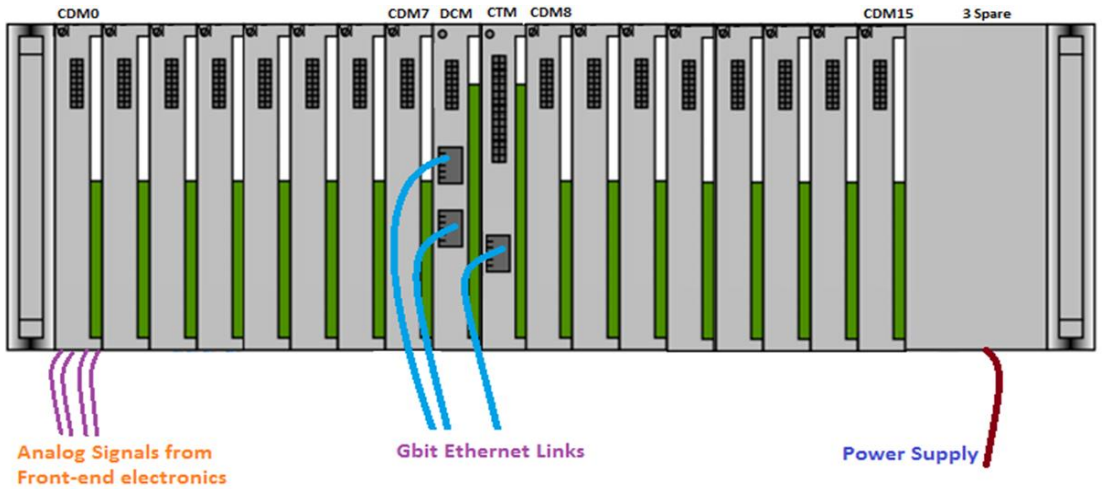
DRS Digitizer Board (DDB)
4 per CDM

Data Concentrator Module (DCM)

Control & Trigger Module (CTM)
1 number

Back-end Module
(233mmx20mmx220mm)





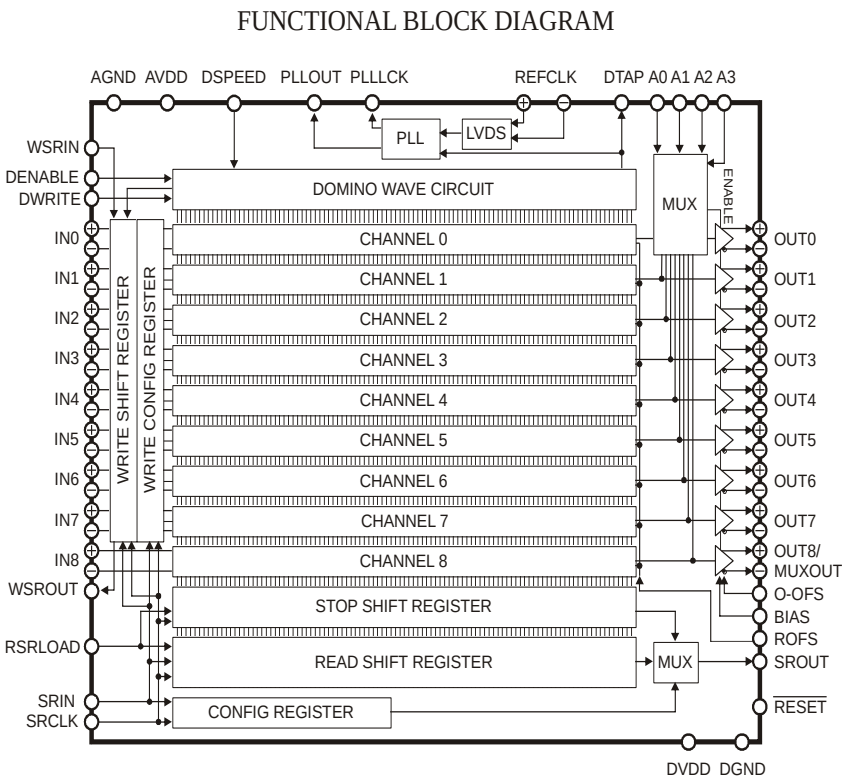
Back-end crate front view

Analog Sampler

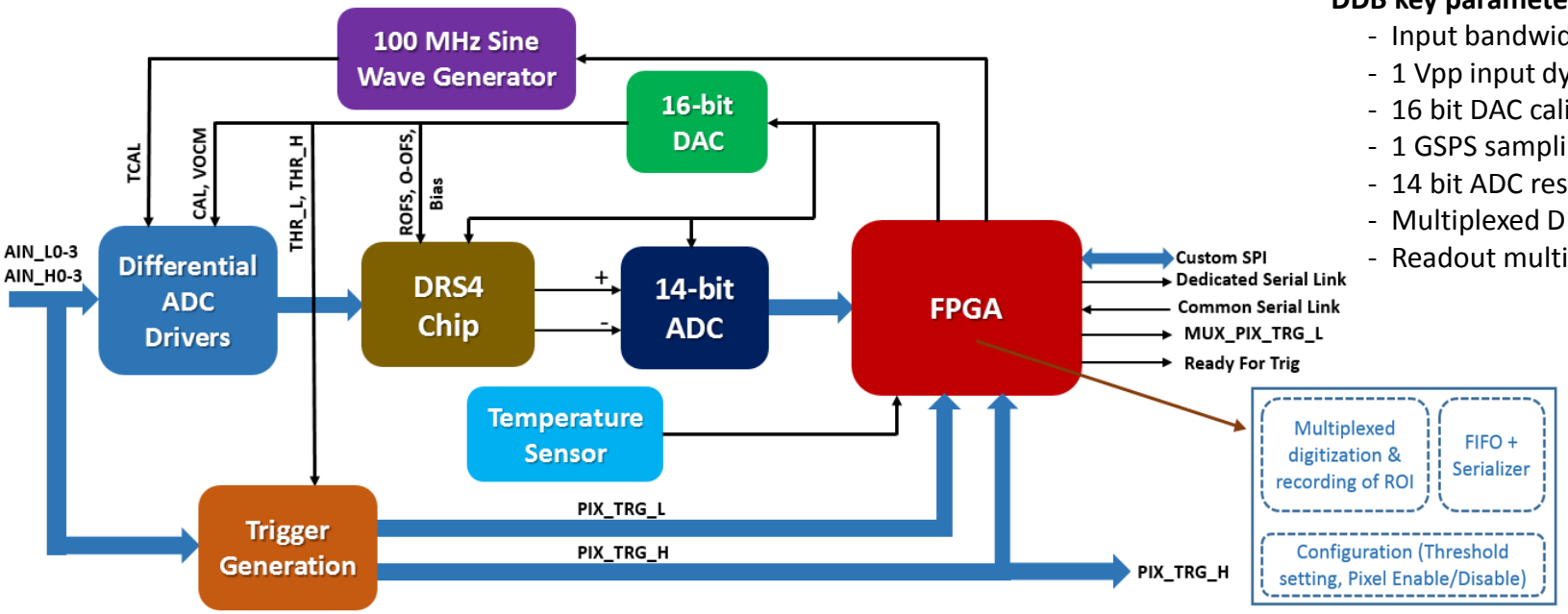
DRS Digitizer Board is designed around an Analog Sampler chip named DRS4.

The DRS4 chip features:

- High channel density: up to 9 channels with 1024 storage cells each
- Differential analog inputs with 950 MHz bandwidth
- 700 MSPS to 5 GSPS sampling speed
- Low noise: 0.35 mV RMS, after offset correction
- Linear In/Out characteristics with 1V dynamic range
- Region of interest readout, dead time proportional to readout depth
- Multiplexed or parallel channel readout
- Low power consumption ~ 140 mW at 2 GSPS
- Channel cascading



DRS Digitizer Board (DDB)



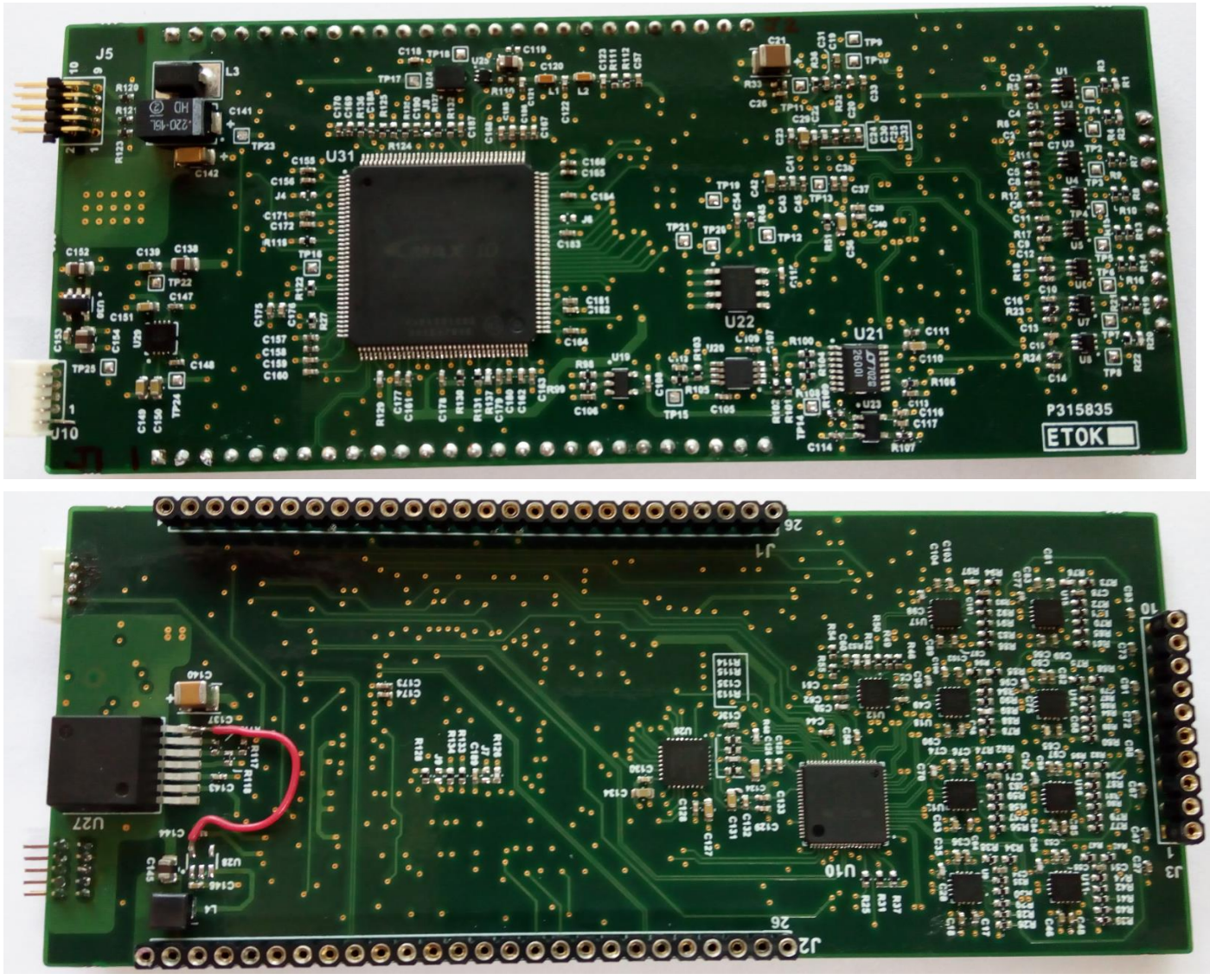
DDB key parameters:

- Input bandwidth 750 MHz
- 1 Vpp input dynamic range
- 16 bit DAC calibration
- 1 GSPS sampling rate
- 14 bit ADC resolution
- Multiplexed DRS4 readout
- Readout multiplexed @33 MHz

Features:

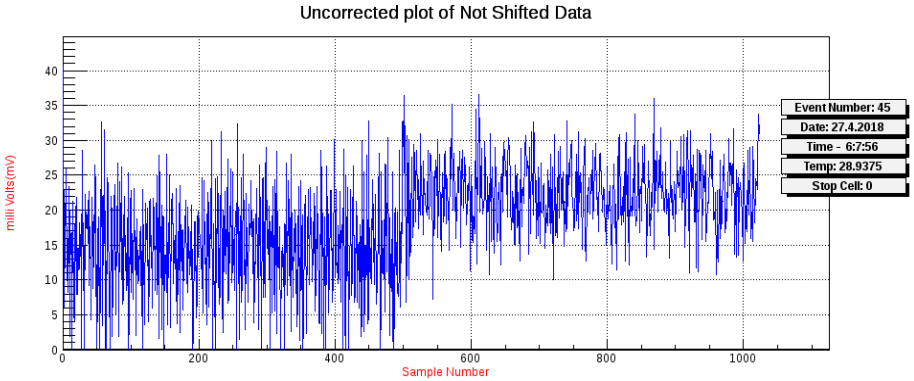
- ✓ It accepts 8 analog single-ended input signals and converts into differential signals
- ✓ High gain input pulse crossing the set threshold generates a pixel trigger whereas Low gain digital pulse is used to recognize high gain saturation channels
- ✓ 9th channel of DRS4 chip used for calibration purpose
- ✓ 32-bit wide, 4K depth FIFO (implemented inside FPGA) for temporary storage of digitized data
- ✓ One common LVDS serial link (@ 20 MbPS) to receive event number and time stamp data from CTM
- ✓ Dedicated LVDS serial link @ 50MbPS for sending digitized data packet to DCM
- ✓ A 16-bit DAC for trigger threshold control, biasing and calibration of DRS4
- ✓ A temperature sensor to monitor ambient temperature
- ✓ Custom SPI link to CDM FPGA for remote control
- ✓ FPGA for overall control and interfacing on-board ICs

DDB Status

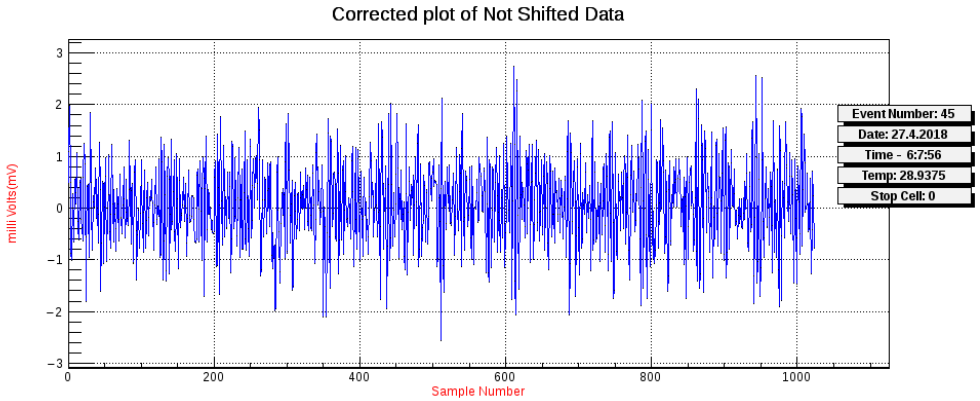


Status: FPGA circuit design for interfacing with all on-board components over. Functionality tests are going on.

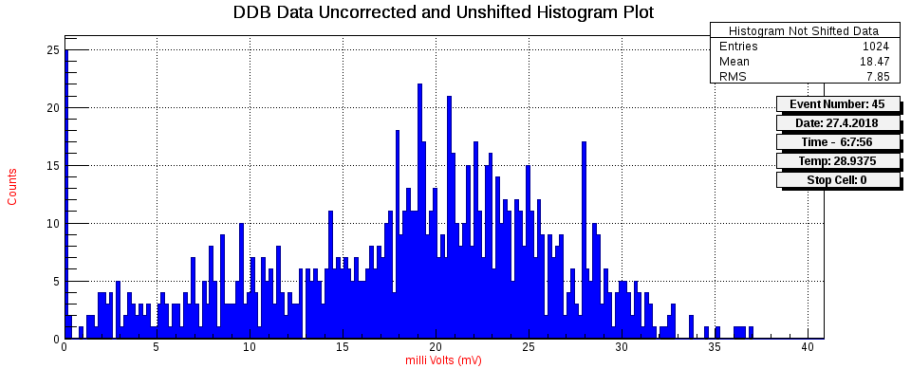
Offset measurements for the DRS4 chip



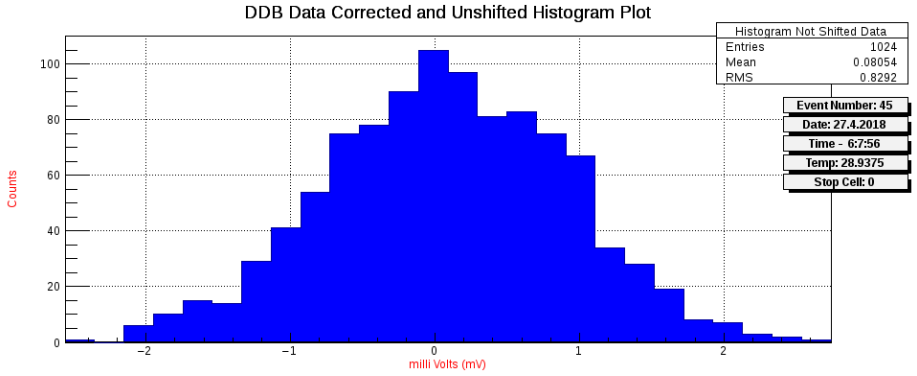
Noise distribution before offset correction



Noise distribution after offset correction

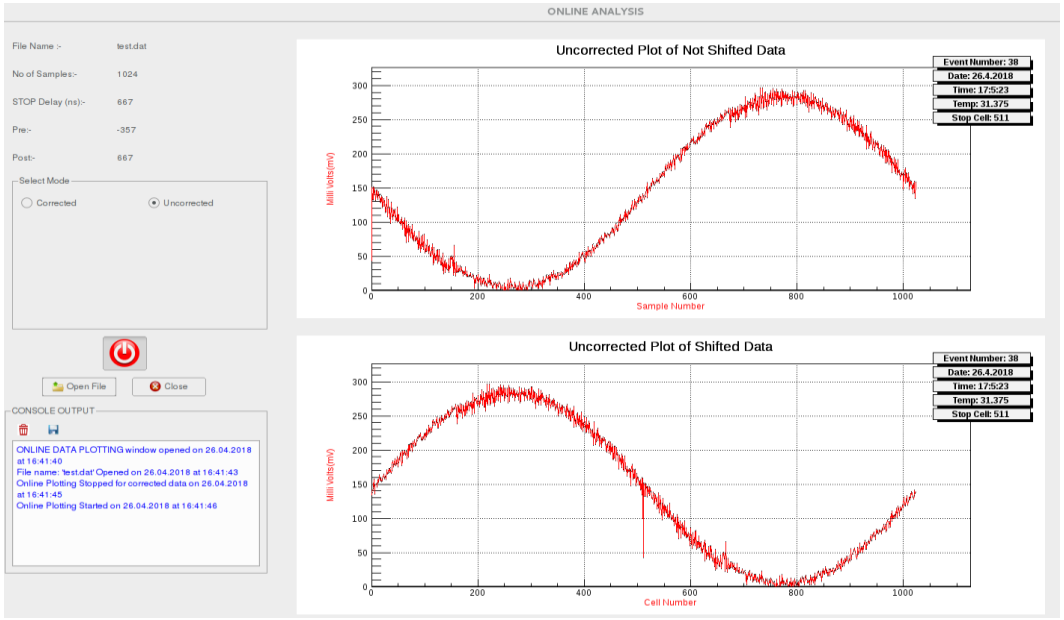


Noise histogram before offset correction

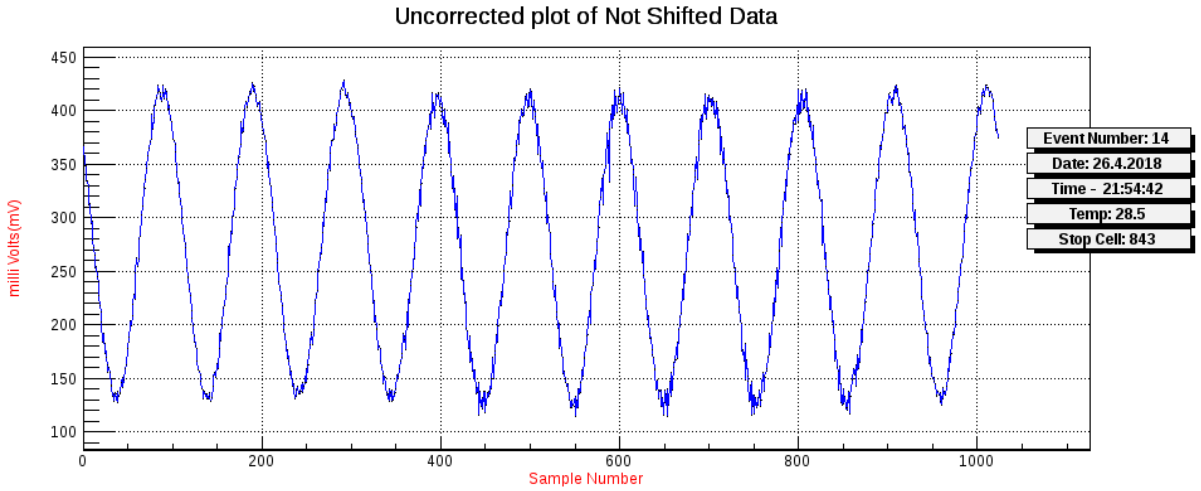


Noise histogram after offset correction

Sine waveforms recorded with DDB



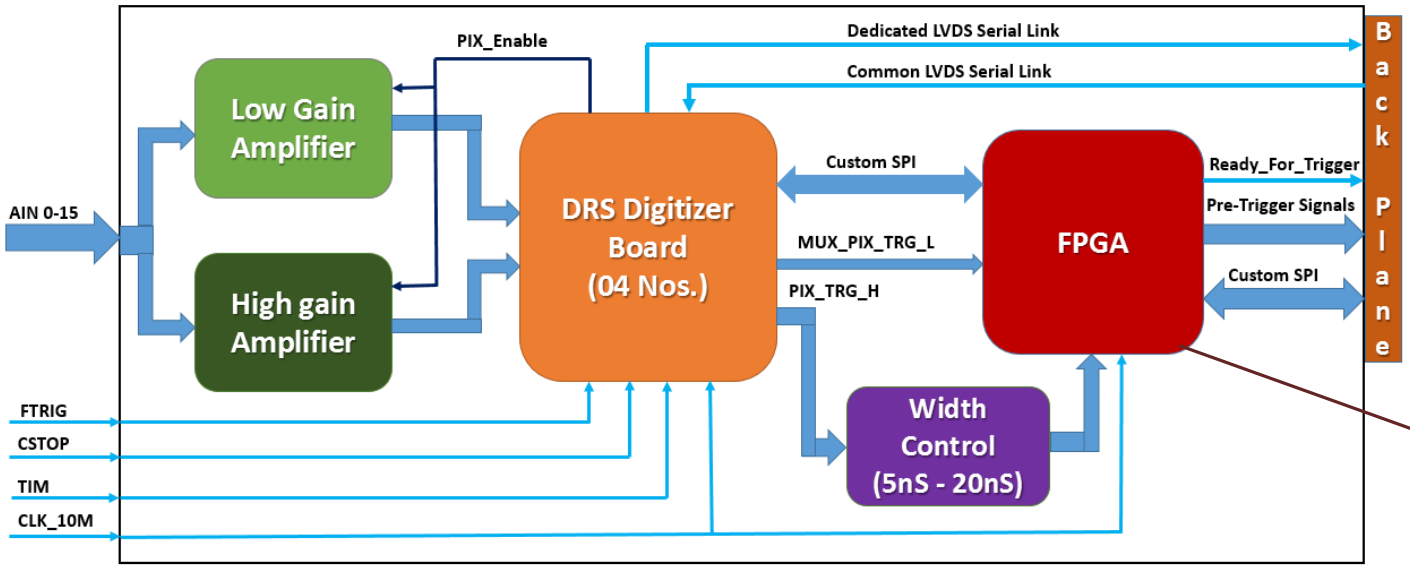
1 MHz Sinewave digitized using DDB

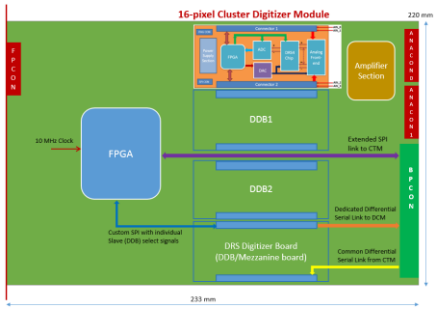


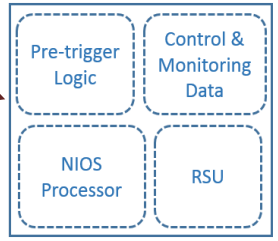
10 MHz Sinewave digitized using DDB

The data analysis software developed using CERN ROOT and Qt

Cluster Digitizer Module (CDM)



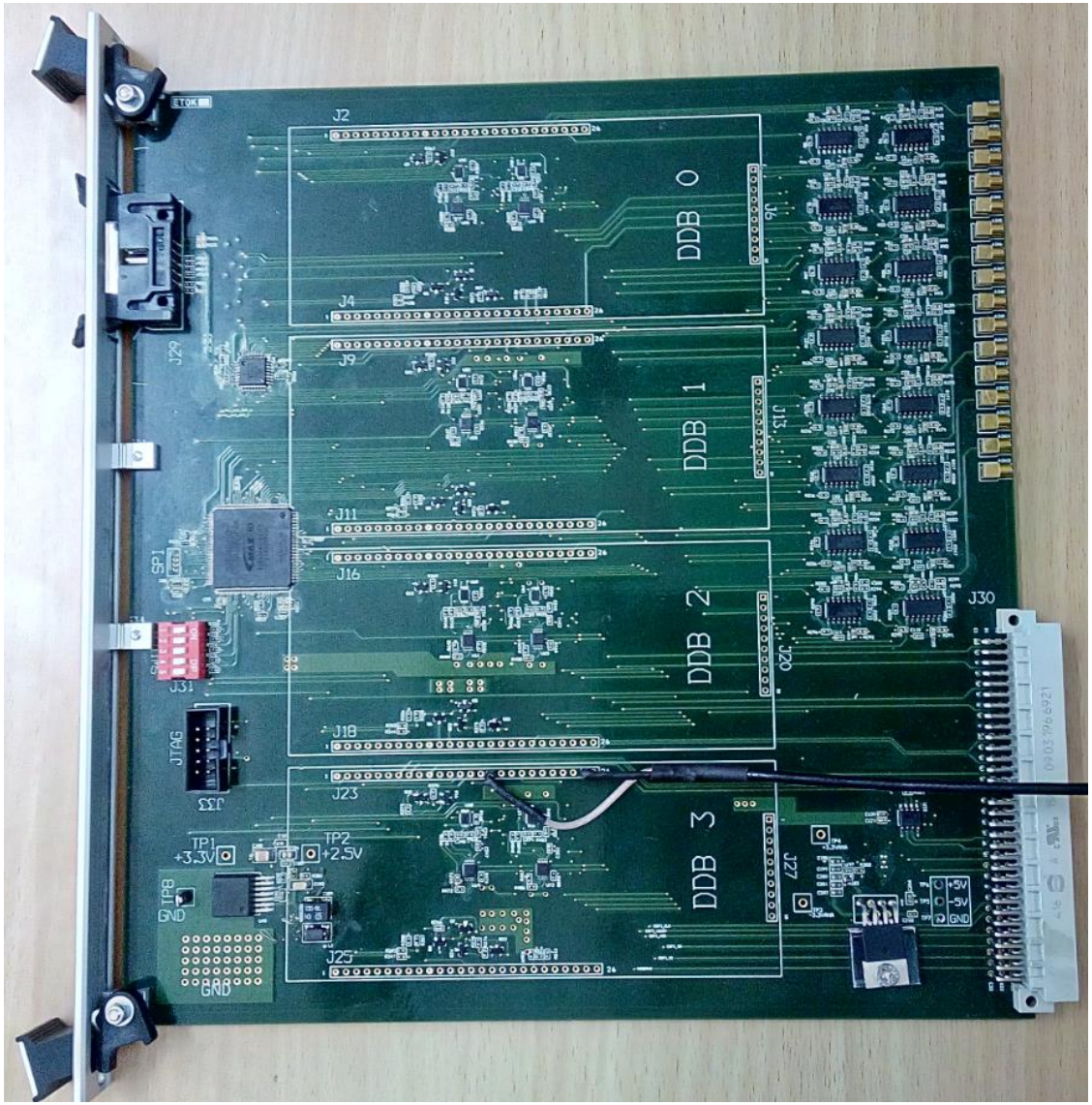




Features:

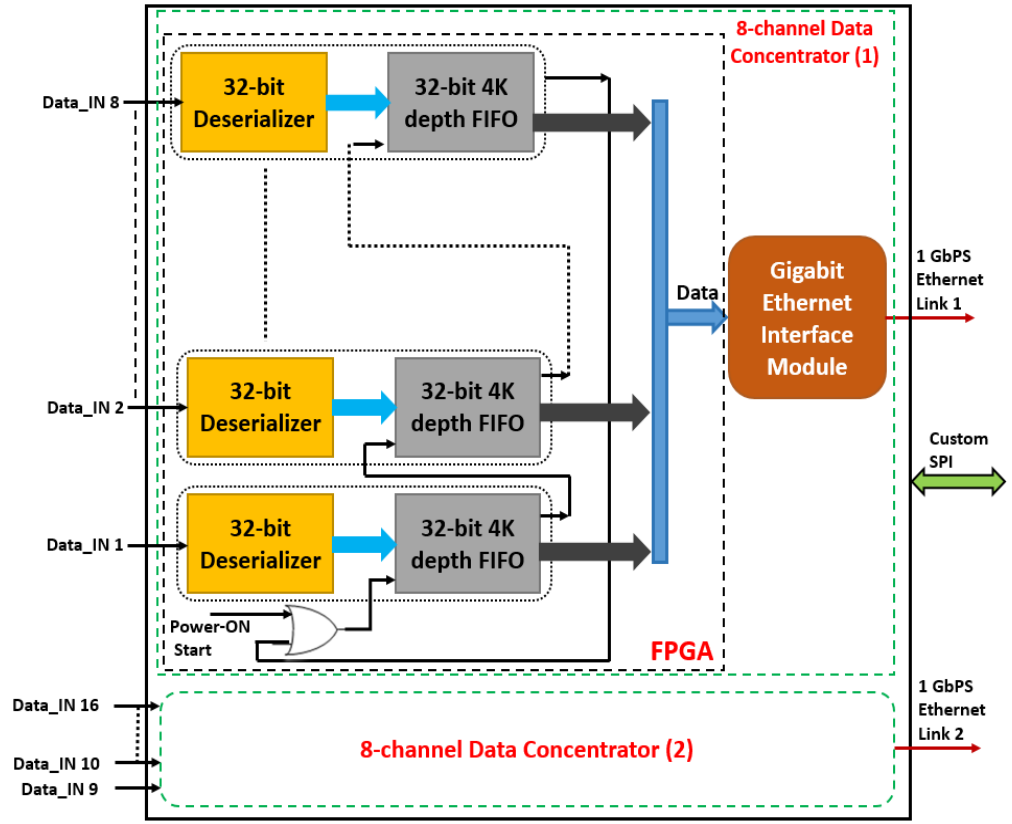
- ✓ The amplifier section generates High Gain (1 - 100 p.e.) and Low gain (1 - 1000 p.e.) version of input analog signals
- ✓ CDM hosts four mezzanine boards called DRS Digitizer Boards (DDBs)
- ✓ Each DDB digitizes eight pulse profiles from 4 pixels (a Low and a High gain version for each pixel)
- ✓ FPGA on motherboard generates various pre-trigger signals (full and partial trigger signals) and Busy signal till digitization completes, communication with on-board DDBs and monitoring, communication with CTM via back plane using custom SPI link
- ✓ Shared LVDS serial link for digitized data transfer to DCM
- ✓ Common LVDS serial link from CTM to receive event marker (event number & time stamp)
- ✓ All CDMs identical and recognized by a 5-bit Module address

CDM Status



Status: CDM PCB assembled. Tested the functionality of on-board components.

Data Concentrator Module (DCM)

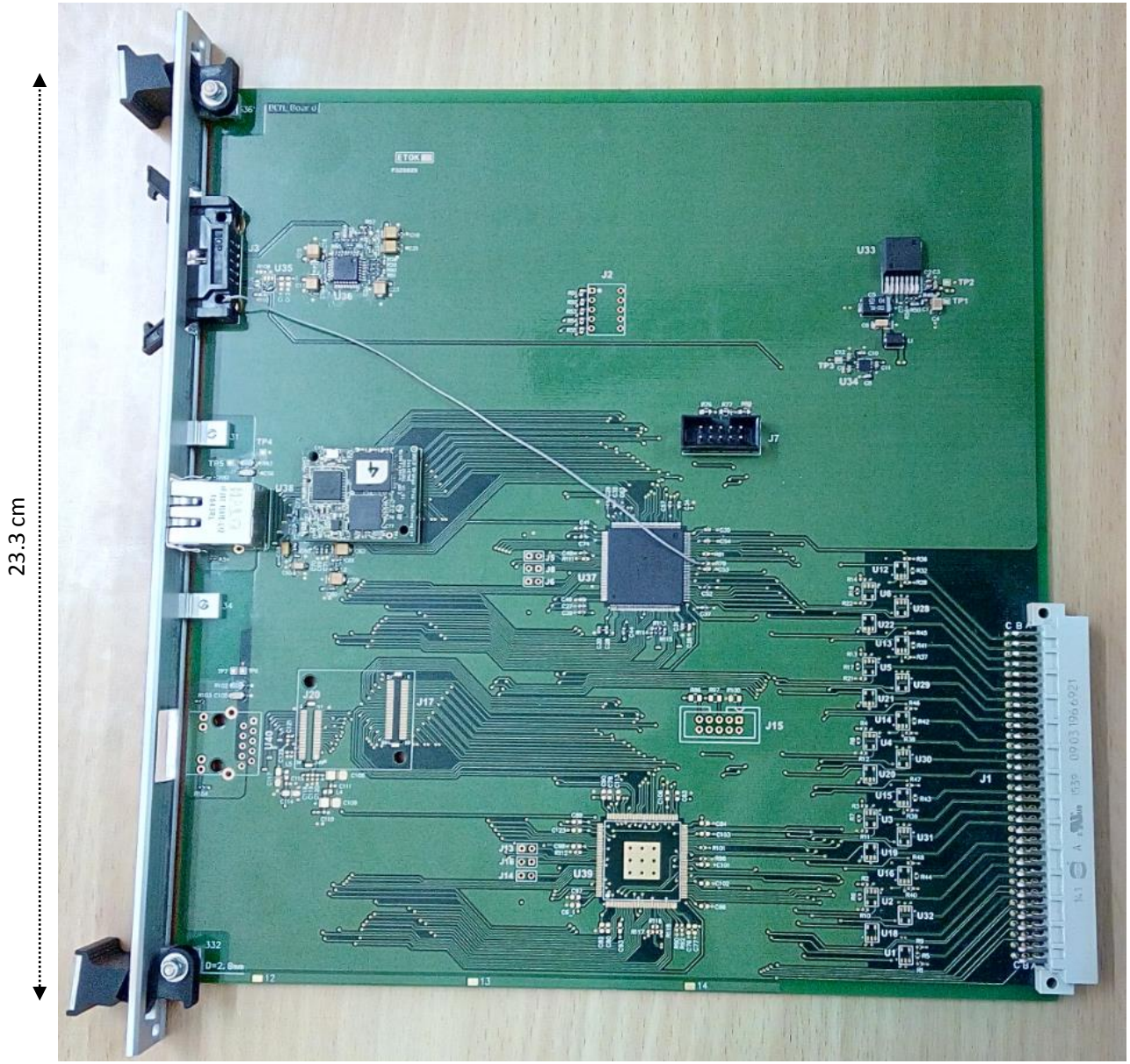


Features:

- ✓ DCM function is to receive the data packets from each of the 16 CDMs over 16 independent LVDS serial links and then transfer the data to remote PC over two 1GbPS Ethernet links
- ✓ DCM consists two identical data concentrator circuits, each serving data transfer for 8-channels
- ✓ DCM communicates with CTM via a custom SPI protocol to receive any initialization or configuration data

Status: The circuit for DCM was synthesized and tested OK for performance on an in-house developed MAX10 FPGA general purpose development board. Data throughput rate of upto 80MBPS is achieved using a test circuit.

DCM Status



Status: 1 section of DCM assembled. Testing in progress.

Control & Trigger Module

Features:

The module has two section viz., Control and Trigger. Each section will have its own FPGA

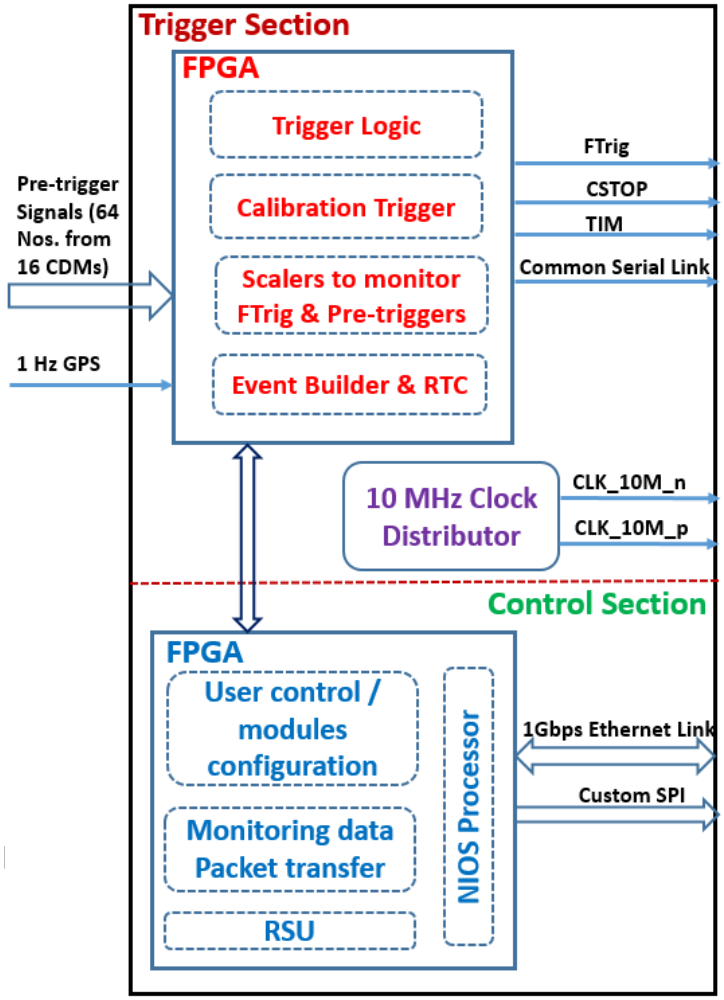
Trigger Section:

- ✓ The trigger section receives pre-trigger signals (a total of 64) from all 16 CDMs and generates a final trigger signal for entire camera
- ✓ Event number with time stamp (100nS resolution + synchronized to GPS) will be sent to all CDMs over a common serial link (20Mbps)

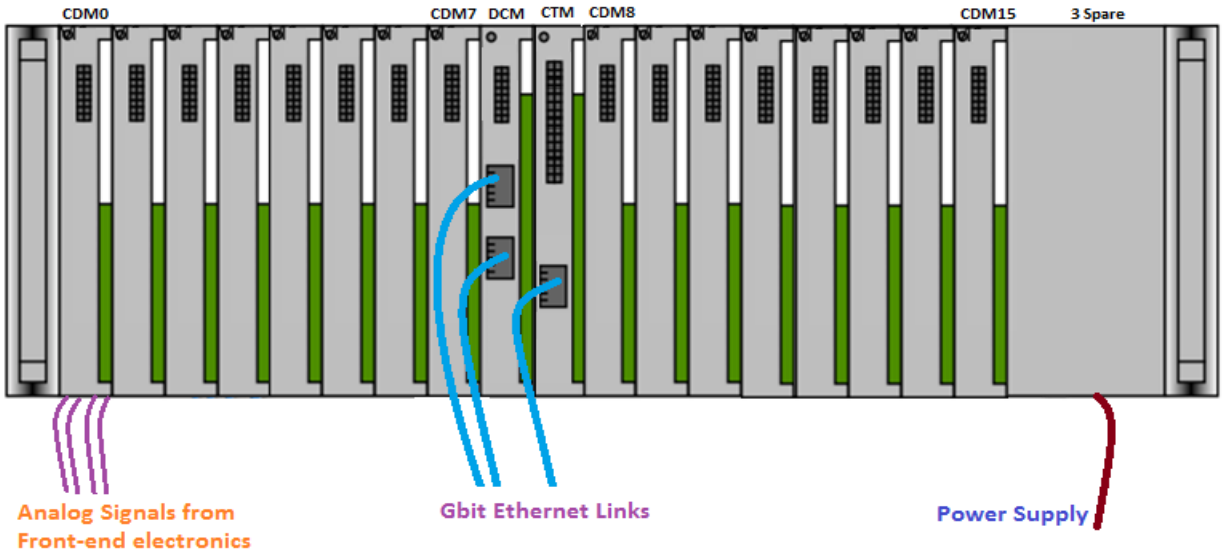
Control Section:

- ✓ The control section will be responsible for sending any control / configuration / initialization data to all other back-end modules. It also records monitor data from all CDMs
- ✓ The control section FPGA will be connected to all other modules through customized SPI (CSPI) link via back plane
- ✓ The control section provides Up/Down Link for all back-end modules to the user
- ✓ The module also provides 10MHz clock signal to all other back-end modules for synchronization of operations

Status: For CTM, the basic up-down Ethernet link between PC & processor is tested OK. The PCB circuit design is in progress.



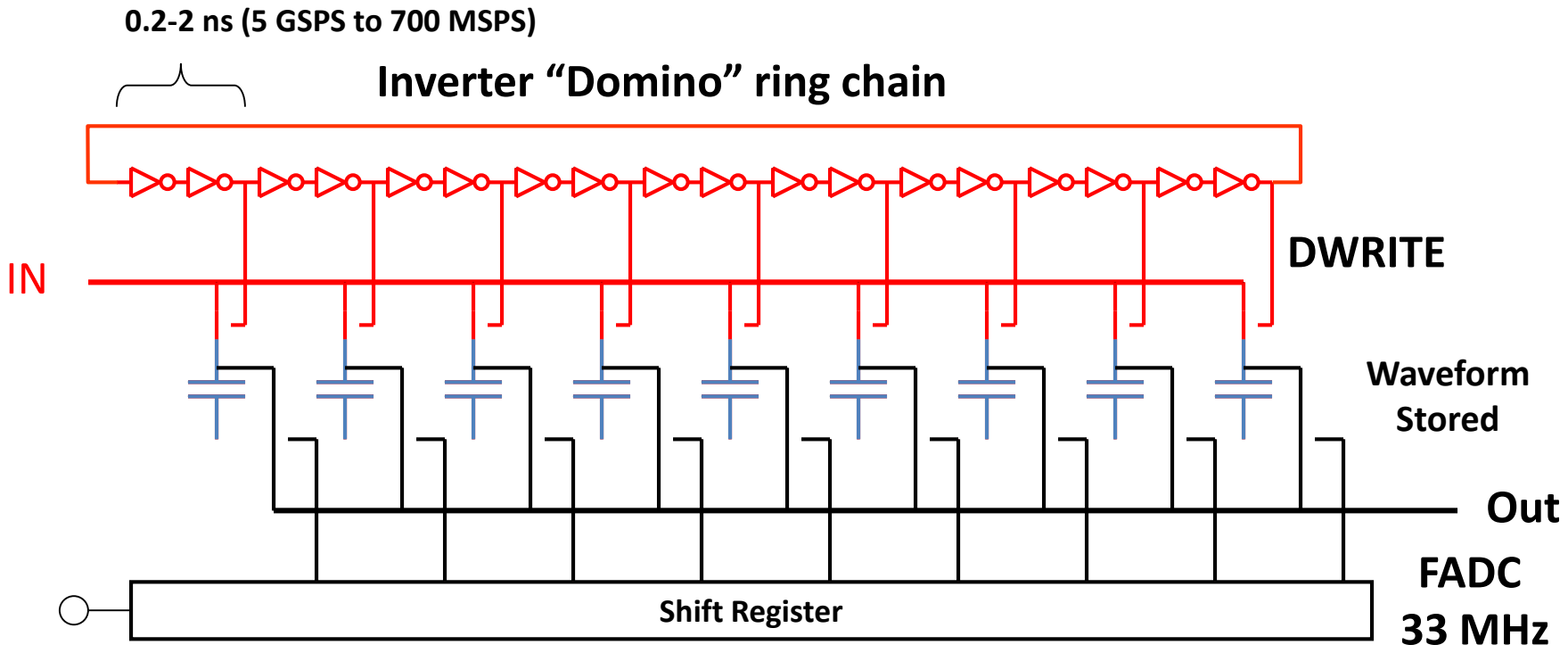
Back-end Crate



Back-Panel PCB: For the back-end crate, the back panel PCB layout was developed. This PCB will cater connectivity between 6 CDMs, 1 DCM & 1 CTM. PCB assembled with crate.

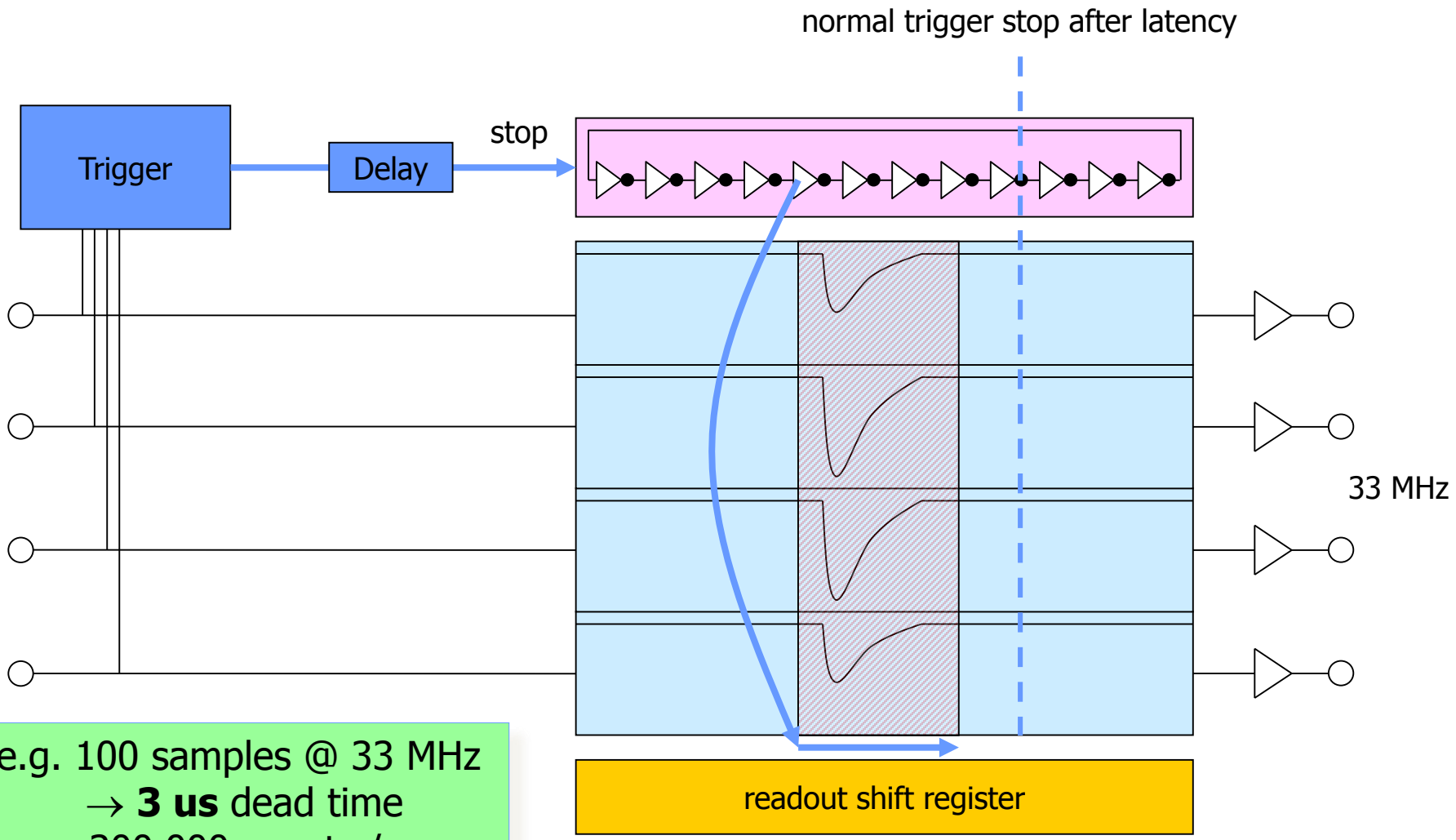
Thanks

Basic Action of Analog Sampler (DRS)



“Time stretcher” GHz → MHz

DRS4 (Analog Sampler) Readout



e.g. 100 samples @ 33 MHz
→ **3 us** dead time
→ 300,000 events / sec